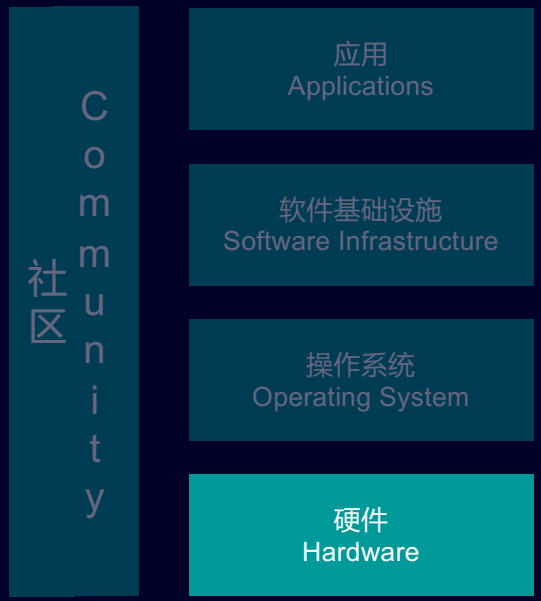
开源EDA Open Source EDA



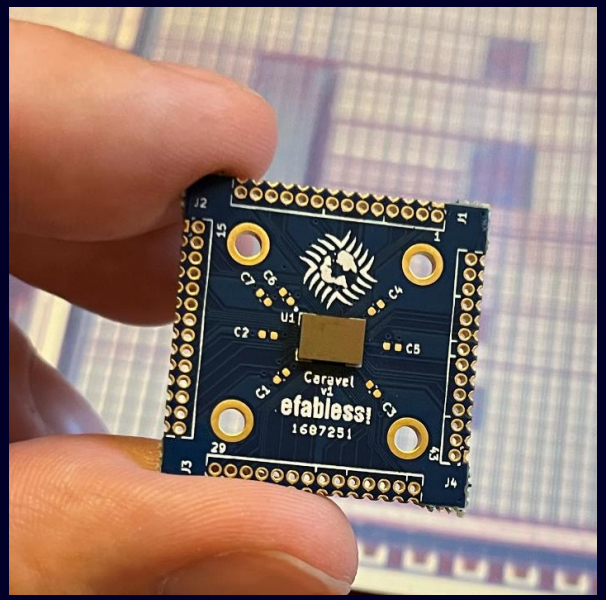
演讲人 Speaker: 李兴权 Li Xing Quan（鹏城实验室 Peng Cheng Lab）

主题 Title: 开源EDA Open Source EDA

内容 Description

谈到开源，半导体是最新的前沿。
近年来，许多EDA工具和IP，如RISC-V，已经变得更为开源。本讲座将介绍iEDA，一个智能的电子设计自动化的基础设施。
Semiconductor is the final frontier when it comes to Open Source.
In recent years a lot of EDA tooling and IP like RISC-V has become open in one or the other way. This talk will introduce iEDA. An intelligent infrastructure for electronic design automation.

我们是如何在西门子开始开源半导体的
How we started at Siemens with Open Source Semiconductors

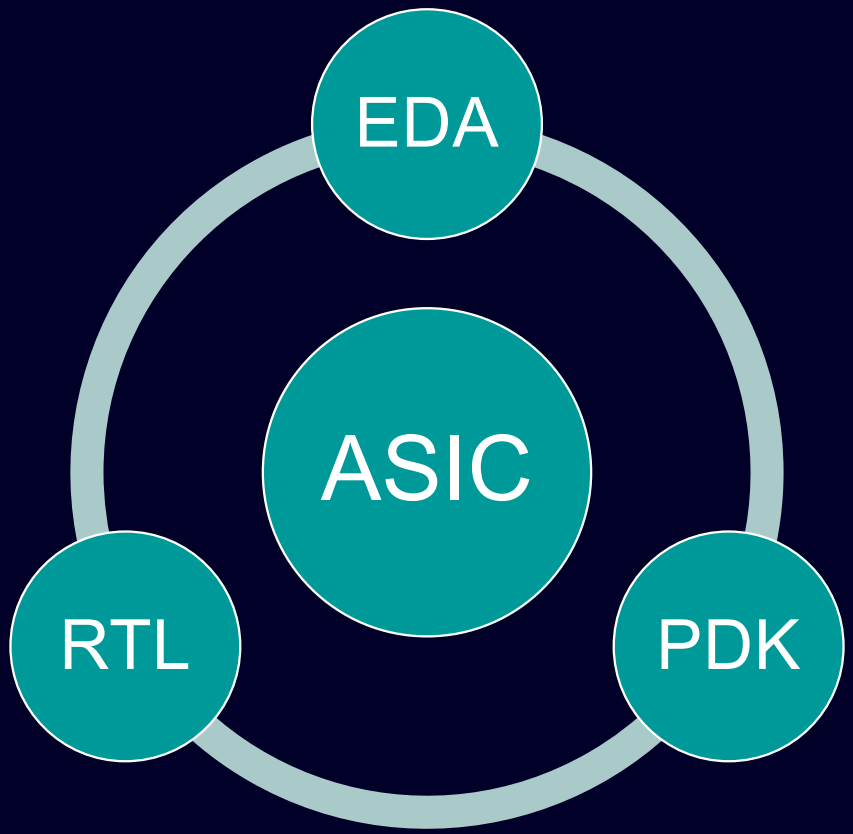


the first “open” tapeout from 2020
2020年后第一次“开源”流片

"*Semiconductors – The Final Frontier Of Open Source*” talk
at the last *Open Source @ Siemens* conference in Zug
“半导体——开源的最新前沿”演讲
在楚格举行的上一届开源@西门子大会上

SIEMENS

我们接下来要做什么
What we wanted to do next



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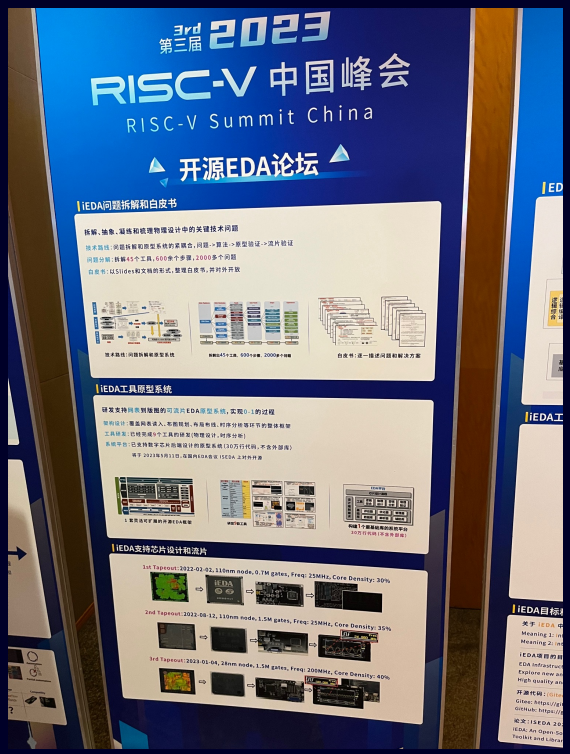
我们在RISC-V中国峰会上的发现
Look what we found at the RISC-V Summit China

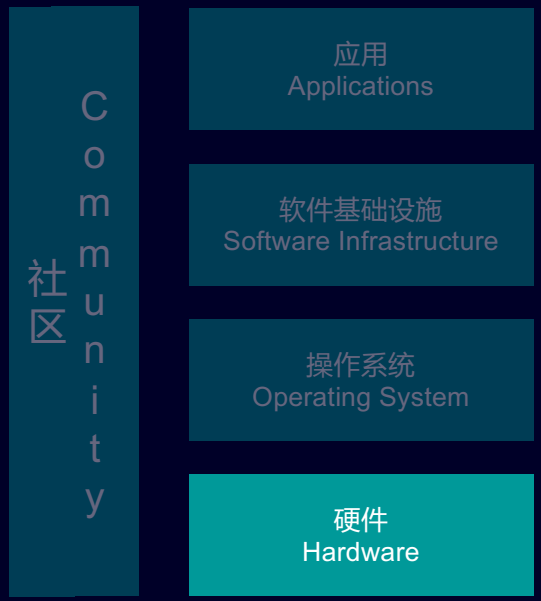
iEDA flow and contributor
iEDA流程和贡献者



iEDA based tapeout
基于iEDA的流片

SIEMENS

开源EDA Open Source EDA



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iEDA: An Open-source EDA Infrastructure and Tool Chain

Xingquan Li（李兴权）

Nov. 29 2023

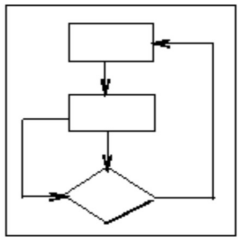
Introduction

iEDA

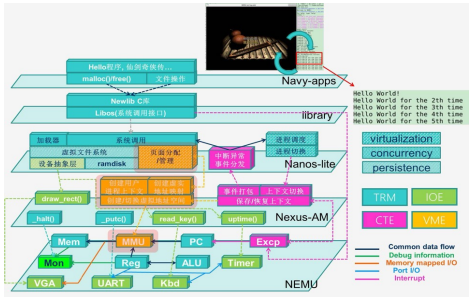
iEDA Application

Chip Design Flow

System Specifications



Architectural Design

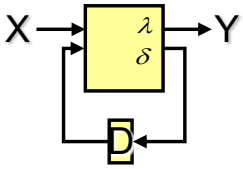


Functional Design

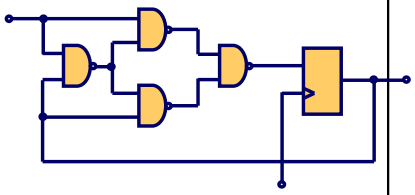
```
module conv;
reg [31:0] m[0:8192];
reg [12:0] pc;
reg [31:0] acc;
reg[15:0] ir;

always
  begin
    ir = m[pc];
    if(ir[15:13] == 3b’ 000)
      pc = m[ir[12:0]];
    else if (ir[15:13] == 3’ b010)
      acc = -m[ir[12:0]];
    ...
```

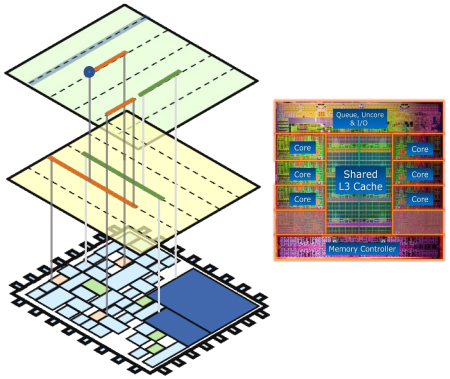
Logic Synthesis



Tech Mapping

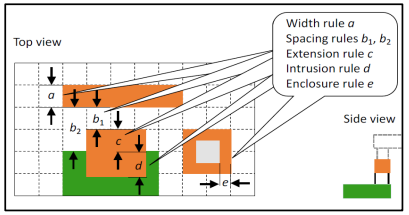


Physical Design

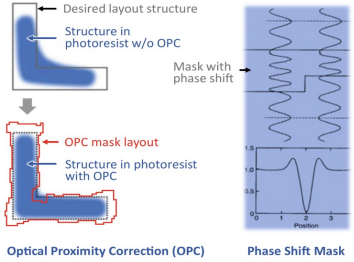


Sign-off Verification

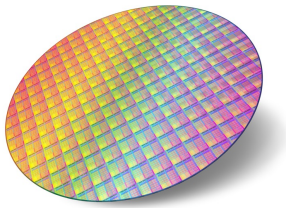
Timing, Power, DRC, ERC, LVS



Layout Processing



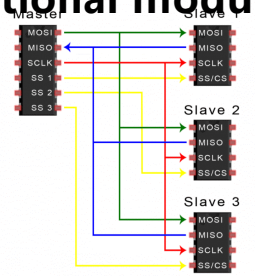
Fabrication

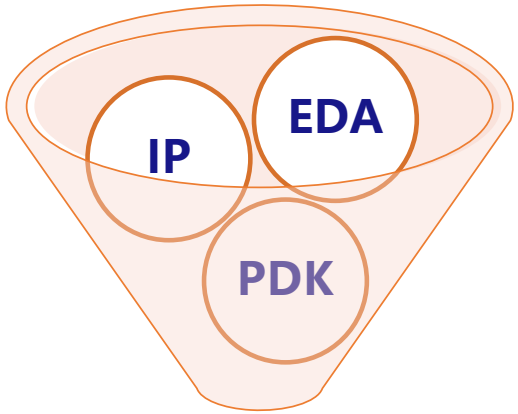


Package and Test

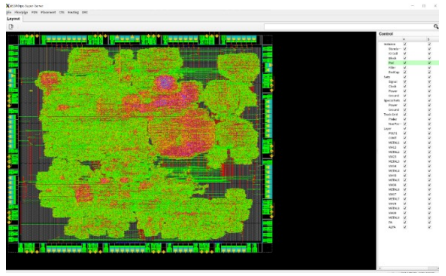
Chip Design Elements

IP: **Intellectual Property**
Functional module

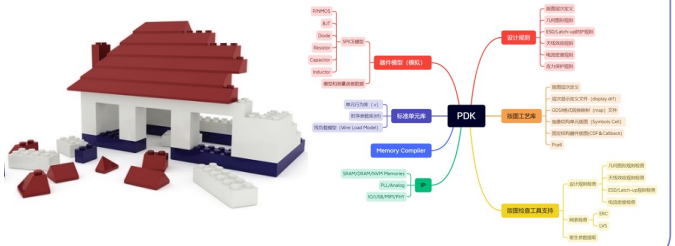




EDA: **Electronic design automation software (tool)**

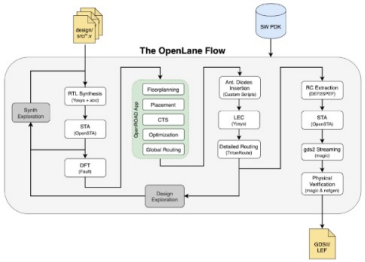


PDK: **Process design kits from foundary**



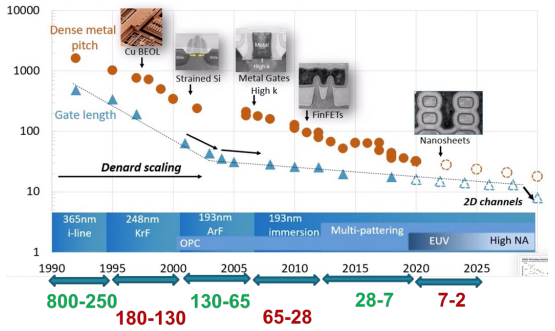
Flow

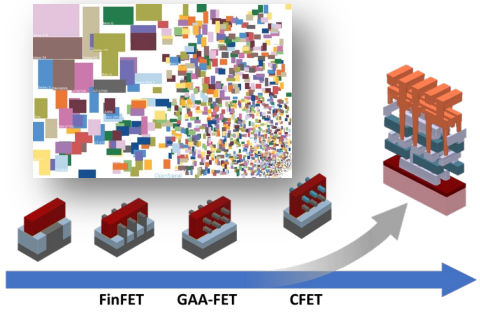
Flow: **Chip design flow config and script**



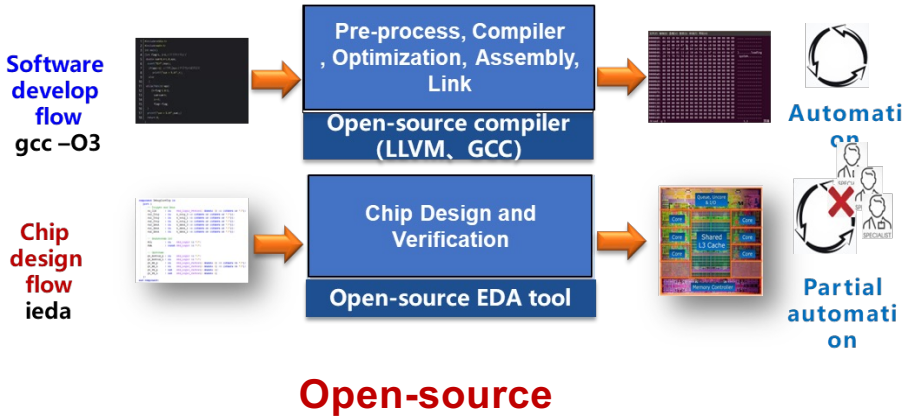
Challenges and Chances

- **Challenges**
  - Moore's Law
  - Gap between academic and industrial
  - Innovation more difficult
  - Design rules are evolving

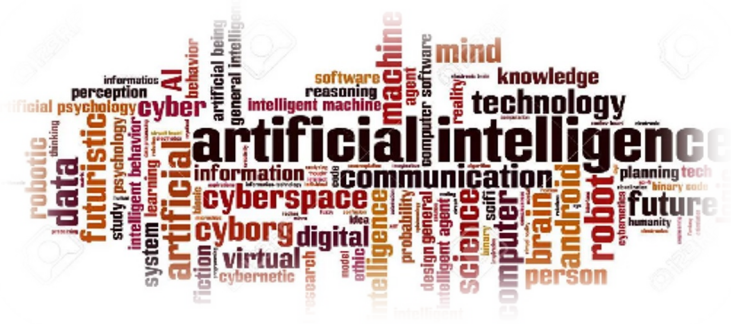




- **Chances**



Open-source



AI

Open-source RTL, PDK and Flow

Open-source RTL

Accelerator	Analog	Connectivity	CPU	FPGA	Memory	System
aes/aes_core	AMS_KGD	aib	OpenXiangShan	FABulous	core_axi_cache	Beagle_SDR_GPS
ara	open-pmic	aib-protocols	a2i	fabric_team	HuanCun	bsg_manycore
FFTGenerator	Analog Basic Blocks/LDO	core_ddr3_controller	black-parrot	OpenFPGA	openram	cep
fpu		HDMI	Cores-SweRV	prga	lake	esp
garnet		i2c	core-v-verif			hero
gplgpu		litedram	cva6			litex
core_jpeg		liteeth	cv32e40p			openFASOC
vortex		litepice	ibex			openpiton
VeriGPU		litescope	microwatt			opentitan
tvm-vta		pymtl3-net	neorv32			openwifi-hw
		verilog-ethernet	picorv32			pulp
		ravenoc	rocket-chip			pulpissimo
		verilog-uart	serv			
			snitch			
			boom			
			Low-RISC			
			OpenXuantie - OpenC910 Core			
			ysyx			

Open-source PDK

PDK name	Process node	Foundary	Institution
Sky130	130nm	Skywater	Google
Sky90	90nm	Skywater	Google
gf180	180nm	GlobalFoundries	Google
NanGate45	45nm	Fake	Si2
Asap7	7nm	Fake	ARM Ltd

Open-source Flow

Flow	Function	Contributor Institution
Qflow	RTL-GDS	Efabless
VSDFLOW	RTL-GDS	VLSI System Design
OpenRoad	RTL-GDS	UCSD
OpenLane	RTL-GDS	Efabless
Ophidian	Netlist-GDS	UFSC
Rsyn	Physical Synthesis	FURG
SiliconCompiler	RTL-GDS	Zero ASIC
iFlow	**RTL-GDS**	**PCL/ICT/BOSC**

Open-source EDA Tools

Design Module	Design Step	Some Commercial Tools			Some Open-source Tools					iEDA
HLS	HLS		Stratus	Catapult Prime	LegUp	GAUT	PandA	FCUDA	XLS	
Simulation Verification	Logic Simulation	VCS	Xcelium	QuestaSim	Verilator	GHDL	FreeHDL	TkGate		
	Circuit Simulation	FineSim/Hspice/CustomSim	Spectre	ModelSim	NGSpice	mixedsim	GnuCap	Qucs	XICE	
	Debug	Verdi/SpyGlass	Indago/litmus	Veloce						
Logic Synthesis	Logic Synthesis	Design Compiler	Genus		Yosys	ABC	EPFL-LS-Lib	LLDHL	UNIVR	iLS
	Tech Map			Oasys-RTL	ABC					iMap
DFT	DFT	DFT Compiler	Modus	Tessent Max	Fault					
Formal	Formal	Formality/CDC	JasperGold							
Physical Design	Partition	Fusion Compiler ICC2 Prime ECO Xtop/Xtime	Innovus	Calibre DesignEnhancer	PartitionMgr	METIS	KaHyPar	MPPart		iNO
	Floorplan				OpenRoad TritonMacroPlacer	OpenRoad	Parquest			iFP
	PDN				OpenPDN					iPDN
	Placement				RePlace OpenDP	DreamPlace	Graywolf	Capo		iPL
	CTS				TritonCTS					iCTS
	Timing OPT				TritonSizer	Gate-Sizing				iTO
	Routing				FastRoute TritonRoute	CUGR Dr.CU	Qrouter	NTHU-Route	BoxRouter/FGR/ORGE	iRT
	ECO				OpenRoad-eco					iECO
Signoff	STA	PrimeTime	Tempus		OpenSTA	OpenTimer				iSTA
	RCX	StarRC	Quantus		OpenRCX	SPEF-Extractor				iRCX
	Power	PrimePower/redhawk	Voltus/Joules	PowerPro/mPower	OpenRoad-pp					iPA
	IR Drop				PDNSim	IREDGe				iIR
Physical Verification	DRC	ICV	Pegasus	Calibre	Klayout	Magic				iDRC
	Antenna				OpenRoad-ant					
	LVS				Netgen					
Validation	Validation	Validator								
Layout Synthesis	MPL			Calibre						
	RET/ILT									
	Mask Generation									

A Promising Open-source Precedent

- **OpenROAD: No Humans, 24 Hours**
- **Efabless-OpenLane: RTL2GDS Digital Flow**

OpenROAD: No Humans, 24 Hours

- **FOCUS: Ease of use and runtime**
- **Directly attack the crises of design and innovation**
  - **Schedule barrier: RTL-to-GDS in 24 hours**
  - **Expertise barrier: No-human-in-loop, tapeout GDS**
  - **Cost barrier: Open source (and, runs in 24 hours)**
- **Unleash system innovation and design innovation**
- **Enable tool customization to system, application needs**

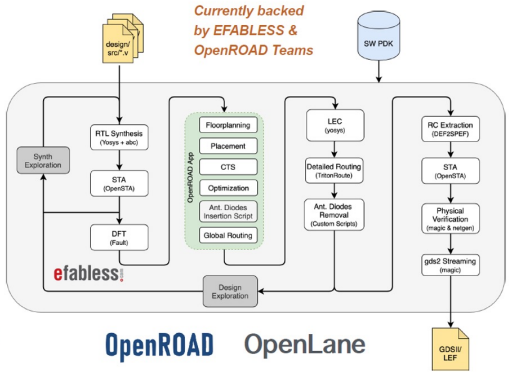
UCSD Qualcomm arm Brown Michigan Minnesota ASU — OpenROAD

Efabless: OpenLane

DIGITAL COMPILER-LIKE RTL2GDS

OpenLane is a no-human in the loop RTL to GDS compiler built around OpenROAD that works like a ***GNU software compiler with trade-offs in area and performance.***

It opens the door for software developers to generate hardware representation without the need for details. **That's at least a 1000X more potential designers!**



Supports SKY130, GF130, XFAB180

12nm support is under development by OpenROAD team

efabless

UCSD Qualcomm arm Brown Michigan Minnesota ASU

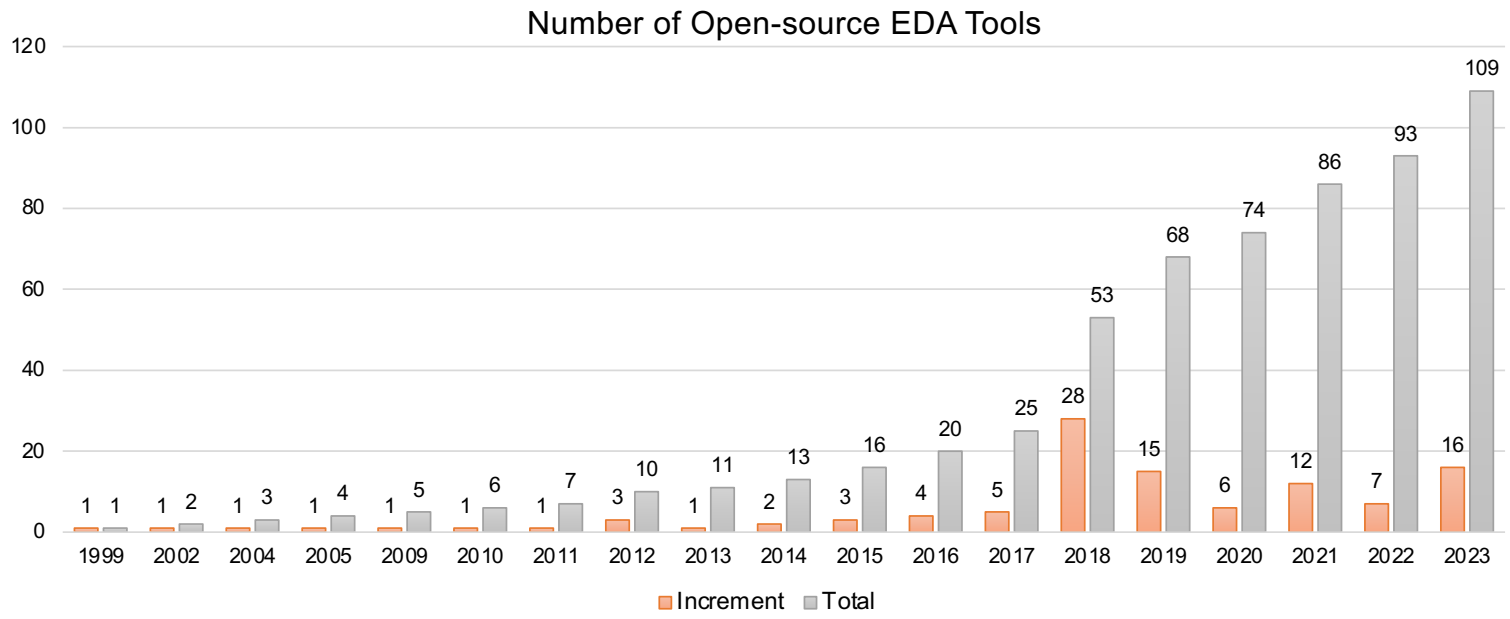
Mohamed Kassem, Efabless

OpenROAD

From "Andrew B. Kahng, The OpenROAD Project: Today and Beyond, 2022"

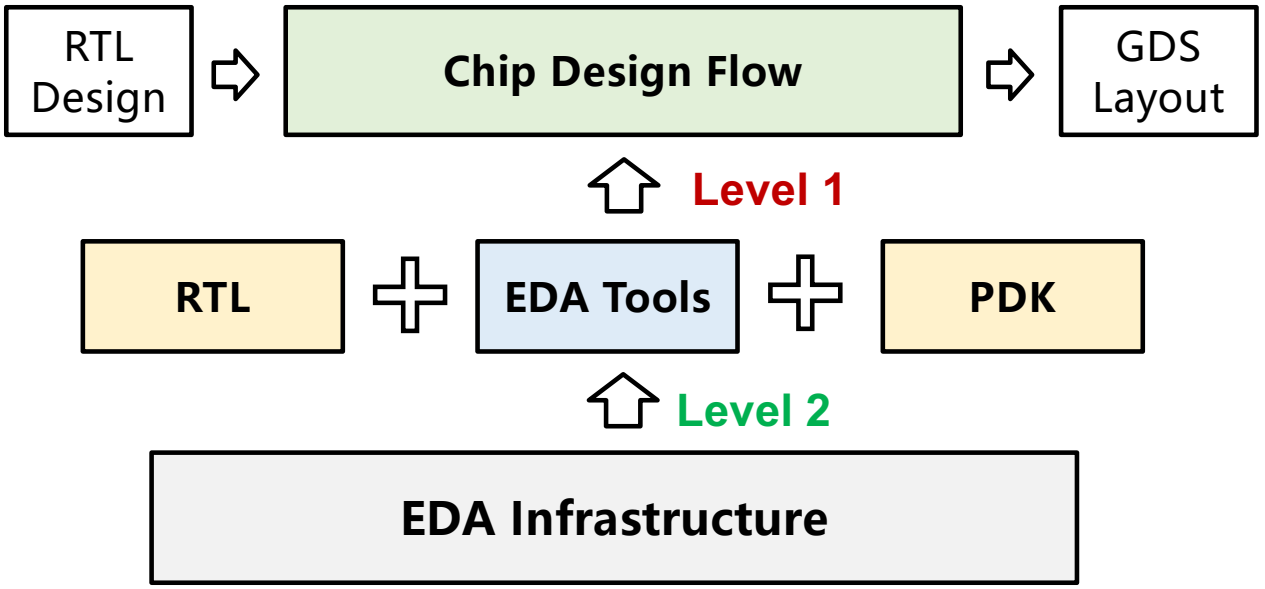
Increasing Open-souce EDA Tools

- Open-souce in EDA may be a tendency



We Need Infrastructure

- **Level 1:** Open-source tools, RTLs, PDKs support chip design
- **Level 2:** Open-source Infrastructure supports EDA, RTL development

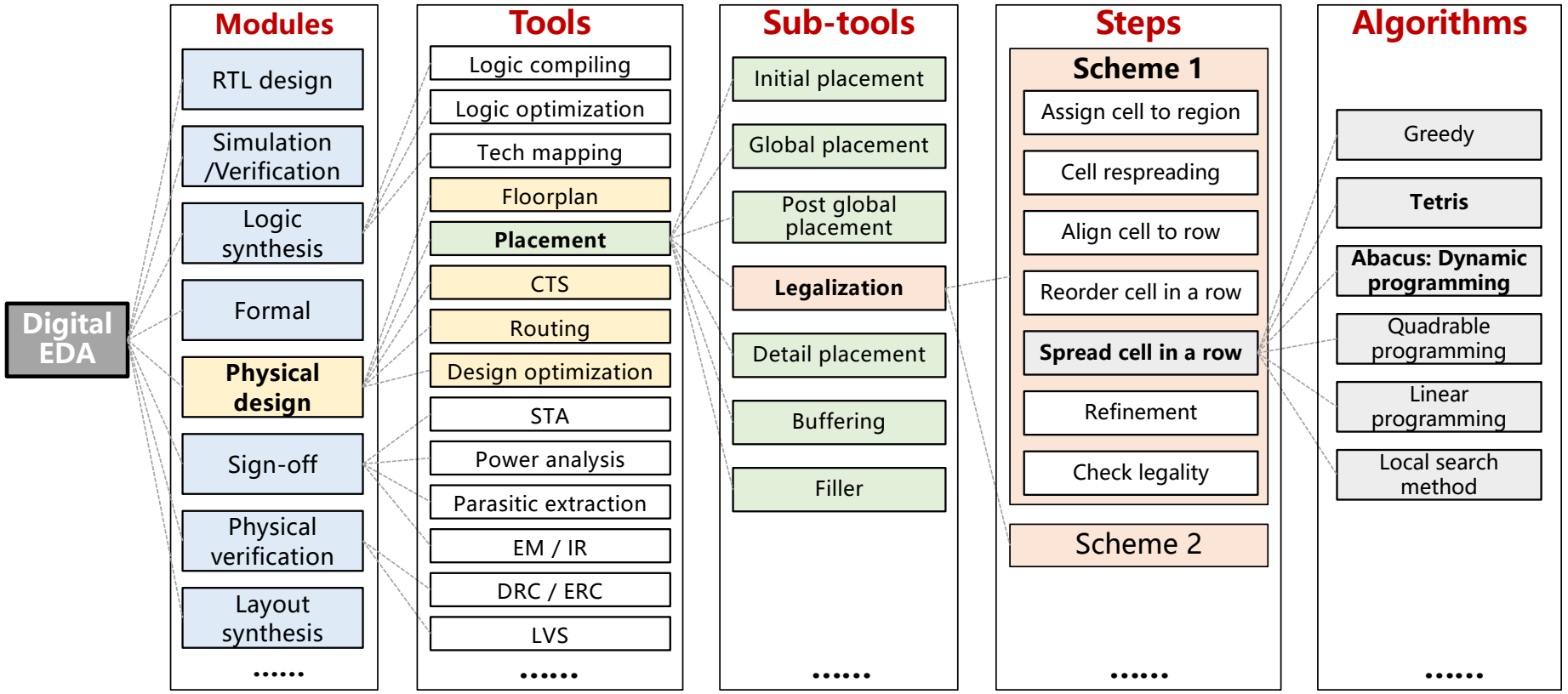


Introduction

iEDA

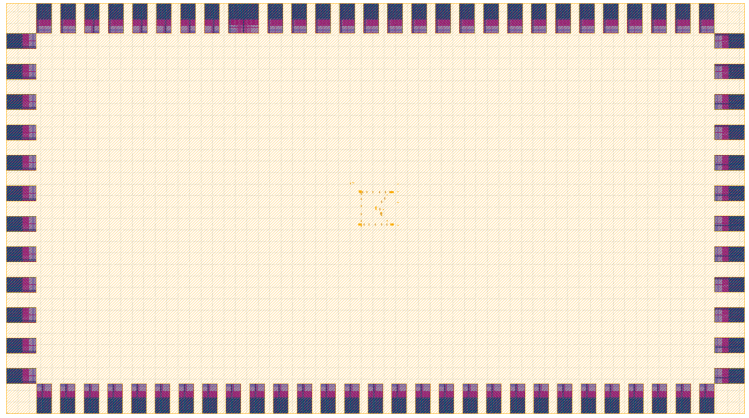
iEDA Application

EDA Decomposition

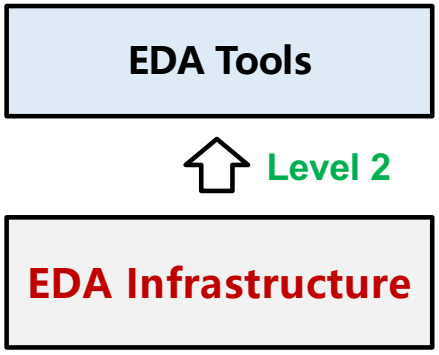


iEDA Introduction

- About “i” in iEDA
  - Meaning 1: Infrastructure
  - Meaning 2: Intelligent
- iEDA Objective
  - EDA Infrastructure
  - Explore new and efficient EDA R&D method
  - High quality and performance EDA tool
- Open-source：(Gitee/Github)
  - Gitee: https://gitee.com/oscc-project/iEDA
  - GitHub: https://github.com/OSCC-Project/iEDA

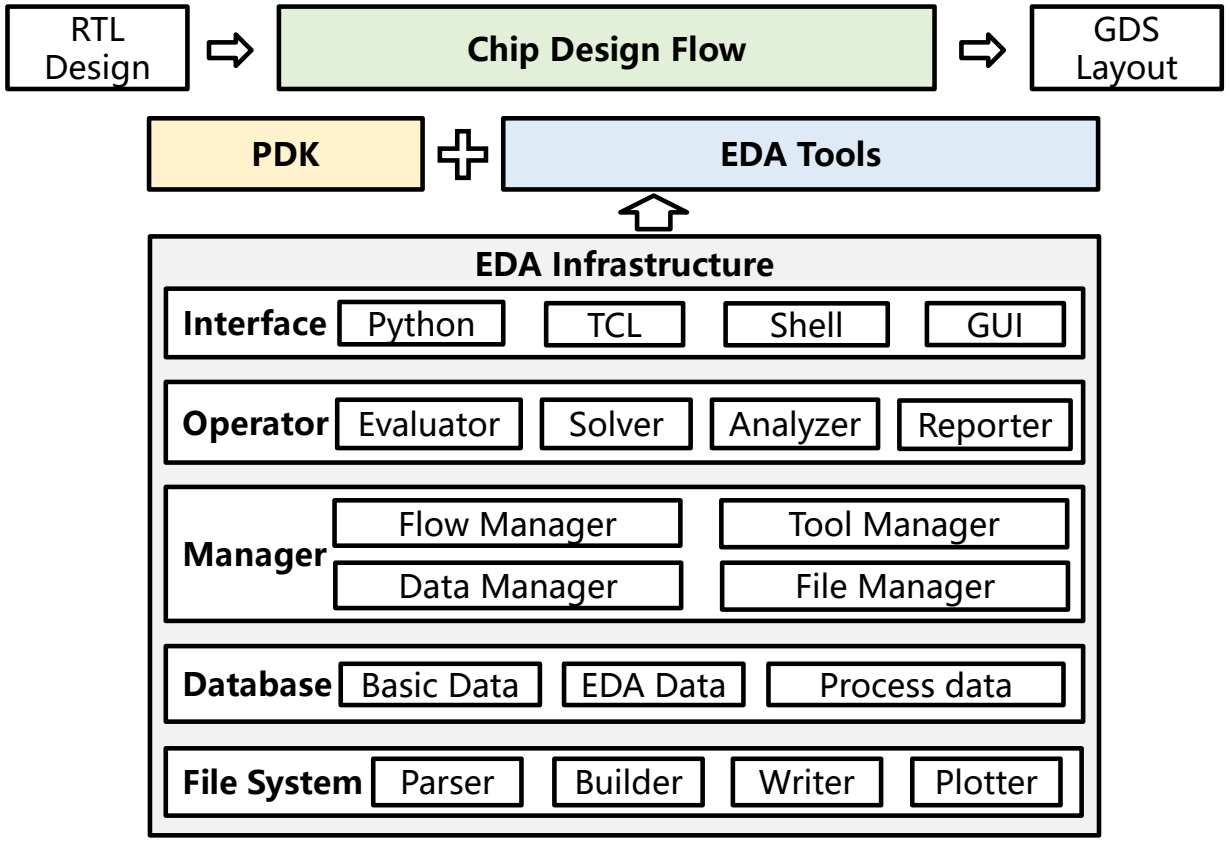


Open-source is not a goal but a way



iEDA-Infrastructure

- File System
- Database
- Manager
- Operator
- Interface
- Utility
- Some perf tools

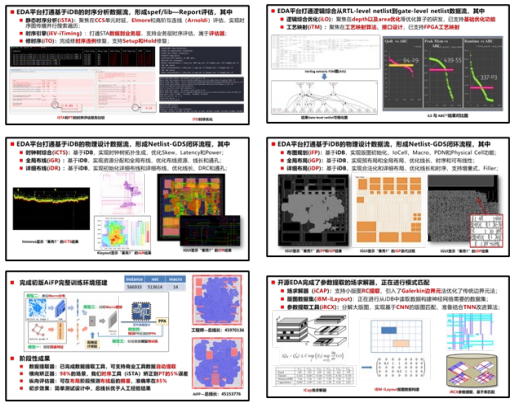


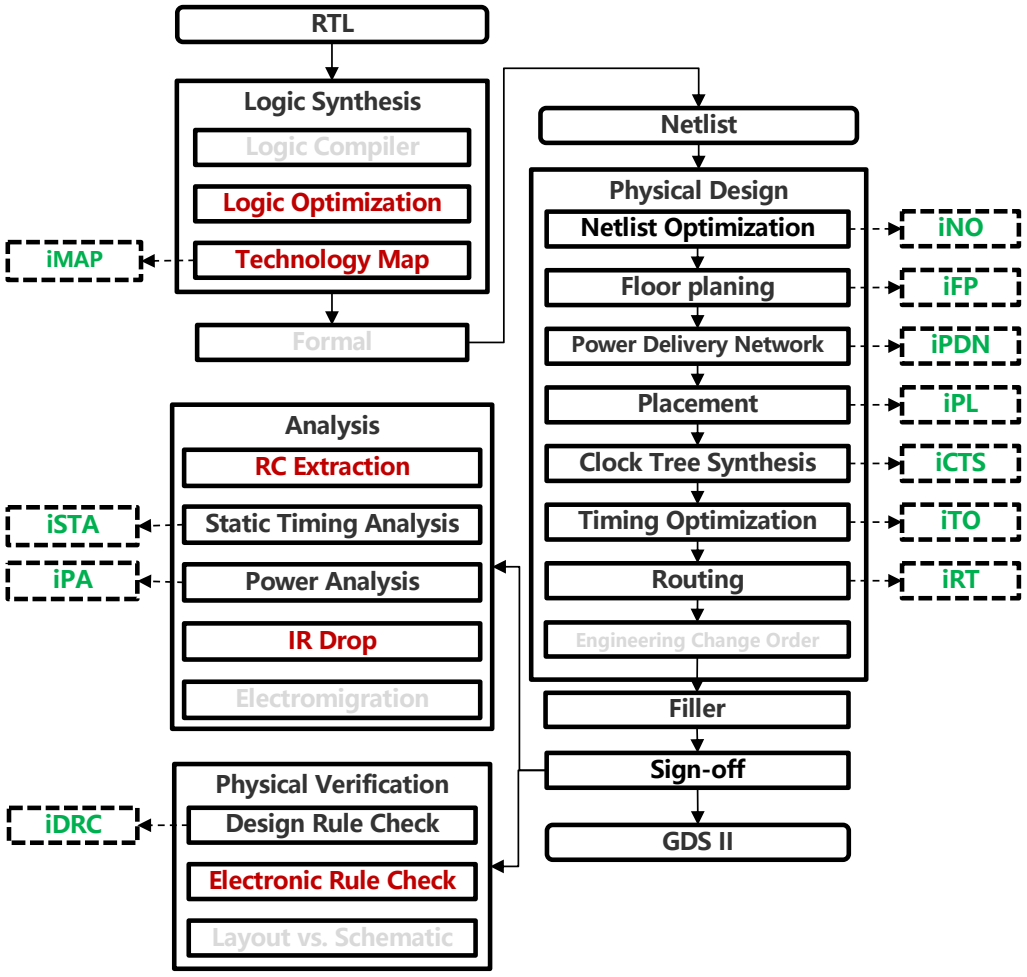
iEDA: Tool Chain

- **AIG/Netlist-to-GDS II**
  - **11 tools, and other 5 tools are R&Ding.**
  - **Design, Analysis, Verification**
- **Design Concept:**
  - **Unified framework, deconstructed and merged**
  - **multi-lingual interface, hot-pluggable modules.**
- **Number of Codes**
  - **>0.3M lines (exclude 3rd party and history)**

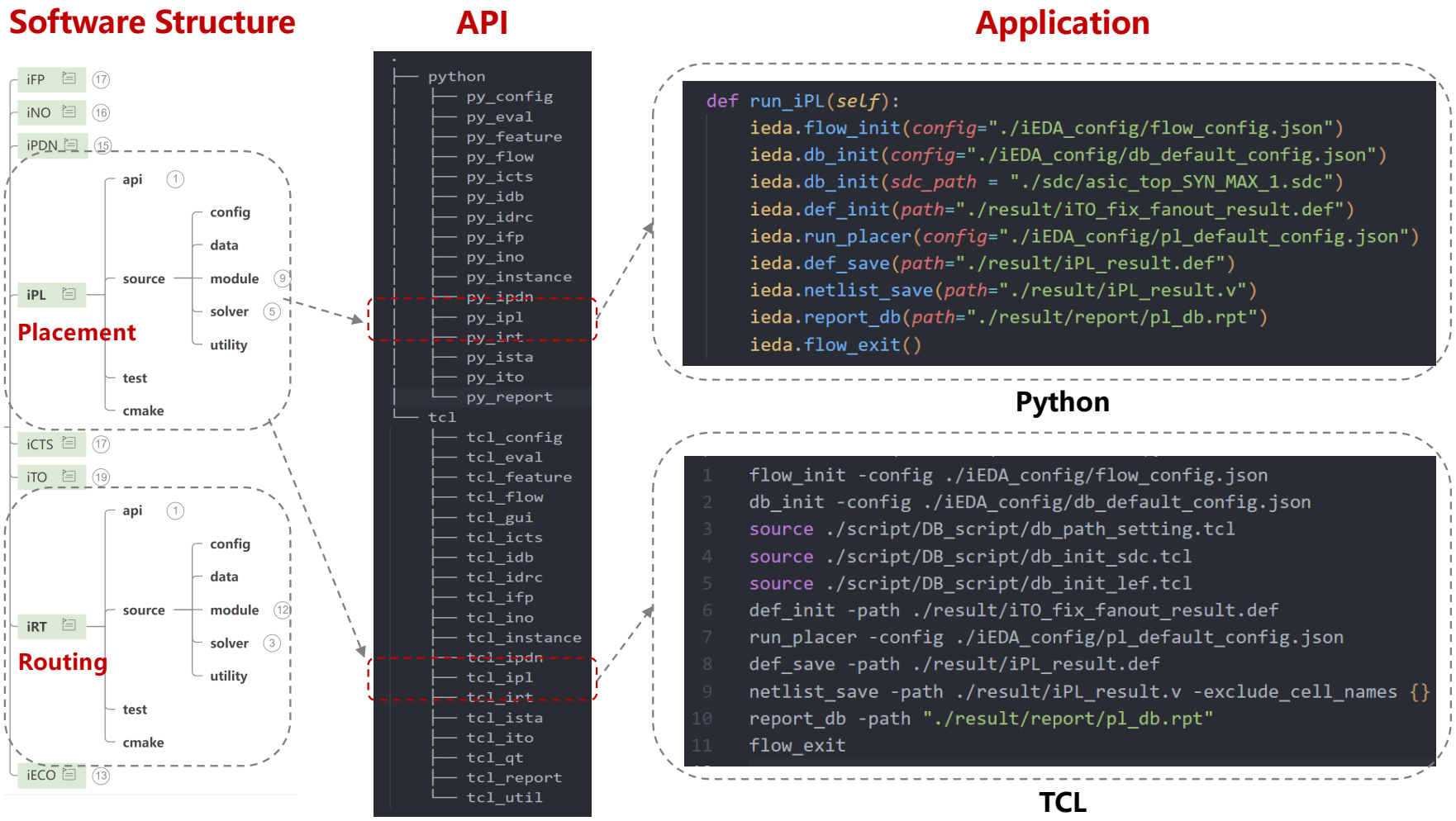
设计模块	设计步骤	iEDA
Logic Synthesis	Logic Synthesis	iLS
	Tech Map	iMap
DFT	DFT	
Formal	Formal	
Physical Design	Partition	
	Floorplan	iFP
	PDN	iPDN
	Placement	iPL
	CTS	iCTS
	Timing OPT	iTO
	Routing	iRT
	ECO	iECO
Signoff	STA	iSTA
	RCX	iRCX
	Power	iPW
	IR Drop	iIR
Physical Verification	DRC	iDRC
	Antenna	
	LVS	

11 Tools



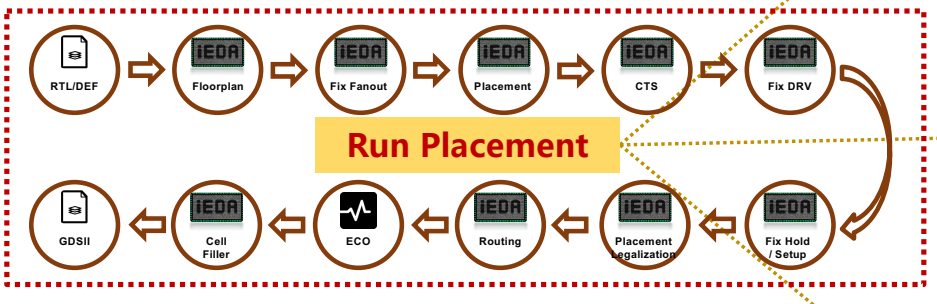


Uniform Software Framework and API



Multiple Programming Language

✓ Support **C++**、**RUST**、**TCL**、**Python**



C++ API

```
/// run placer
if (PLFConfig::getInstance()->is_run_placer()) {
  if (tmInst->autoRunPlacer(PLFConfig::getInstance()->get_ipl_path())) {
  }
}
```

TCL API

```
#============================================================
##   read def
#============================================================
def_init -path ./result/iTO_fix_fanout_result.def

#============================================================
##   run Placer
#============================================================
run_placer -config ./iEDA_config/pl_default_config.json
```

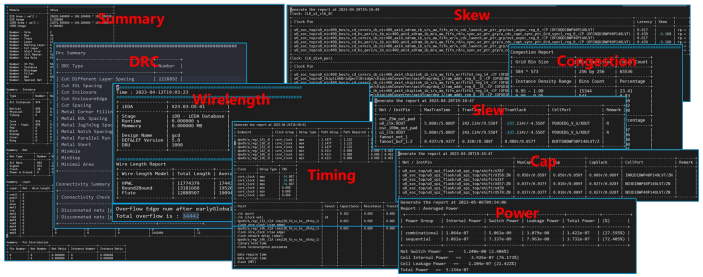
Python API

```
def run_placer(self, input_def : str):
    self.read_def(input_def)

    path = self.path_manager.get_workspace().get_config_ieda(FlowStep.place)
    ieda.run_placer(path)
```

Multiple Data Analysis and Debug Methods

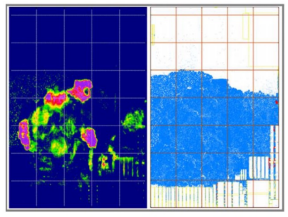
Report

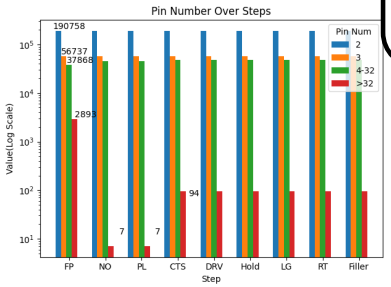


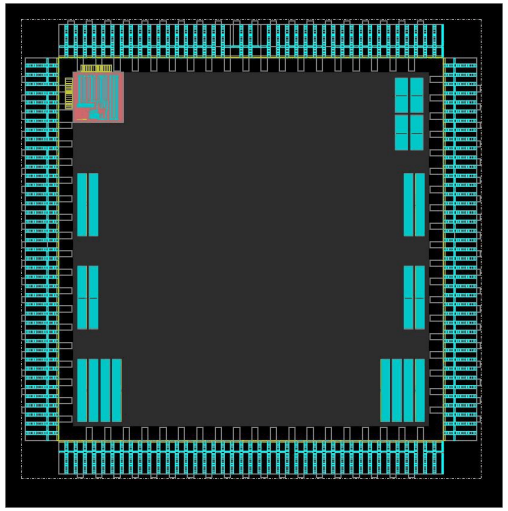
Log

Report | Log | Chart | GUI

Feature Chart







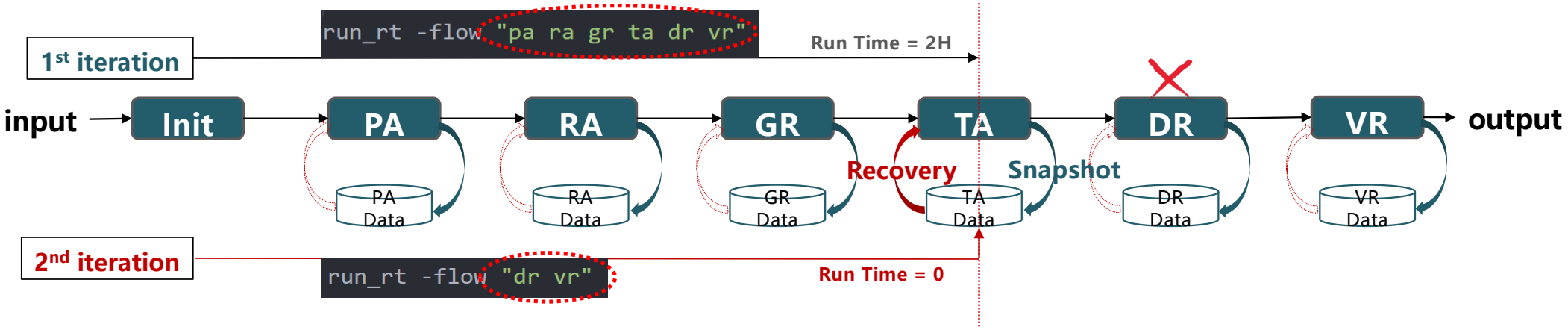
GUI

Data Snapshot & Recovery

- iEDA adopts **serialization and deserialization** to achieve data snapshot and recovery:

Data Snapshot
- Tool Process Data
- Result Data
- Algorithm Data

Data Recovery
- Tool Process Data
- Result Data
- Algorithm Data

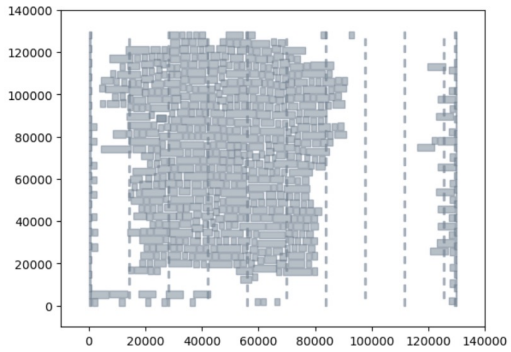


Evaluation: Horizontal Comparison

- Compare and analyze the Q&R of designs, tools, algorithems and flows

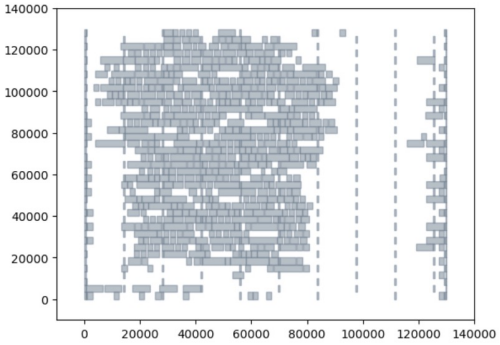
design	aes	aes_core
PDK	sky130	sky130
instance area	408034.7568	371050.9776
IO pin	76	520
instances	45854	42044
nets	30634	28536
core_area	1352765.88	1230601.766
total wire length	2695657	2809505
total vias	280870	271884
setup_slack (max)	14.7	14.73
hold_slack (min)	0.22	0.4
suggest freq (MHz)	188.6792453	189.7533207

Design Comparison

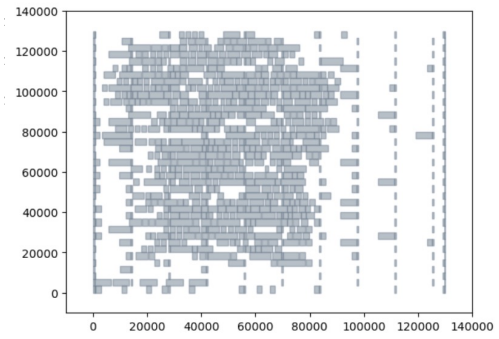


Input

Metrics	Abacus	Tetris
Input HPWL	10127910	10127910
Legal HPWL	10426323	11276288
Detailed HPWL	9901517	10214554
Total STWL	10637190	10950590
Max STWL	431085	435825
Total Movement	795829	2183285
Total Time (s)	0.005505	0.000937



Abacus

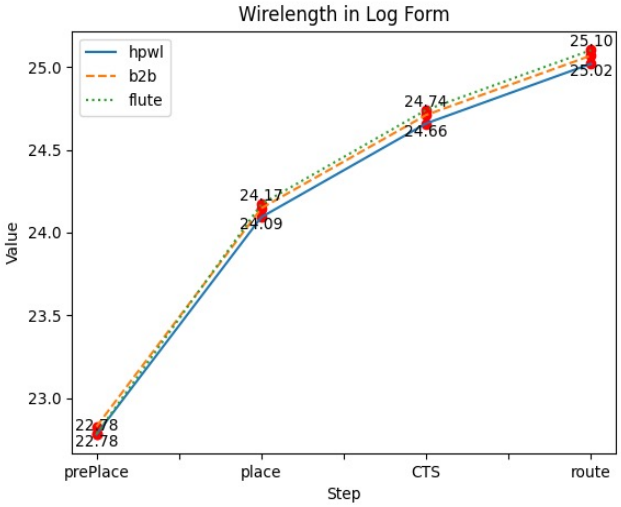


Tetris

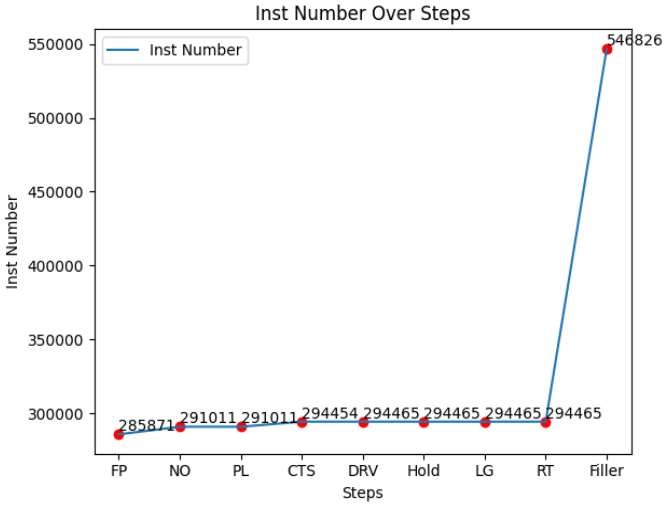
Algorithm Comparison

Evaluation: Vertical Comparison

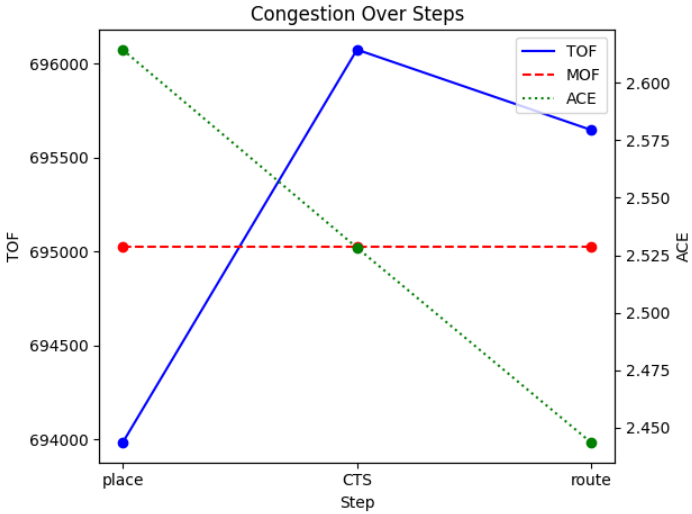
- Analyzing the numerical changes of an indicator **across different stages**
- Differences from: 1) data change, and 2) differences evaluation models
- Uasage：evaluating the design quality, analyzing the margin, and optimizing collaboratively



Wirelength



#Instances



Congestion

Rich API and Documentation

C++ API Doc

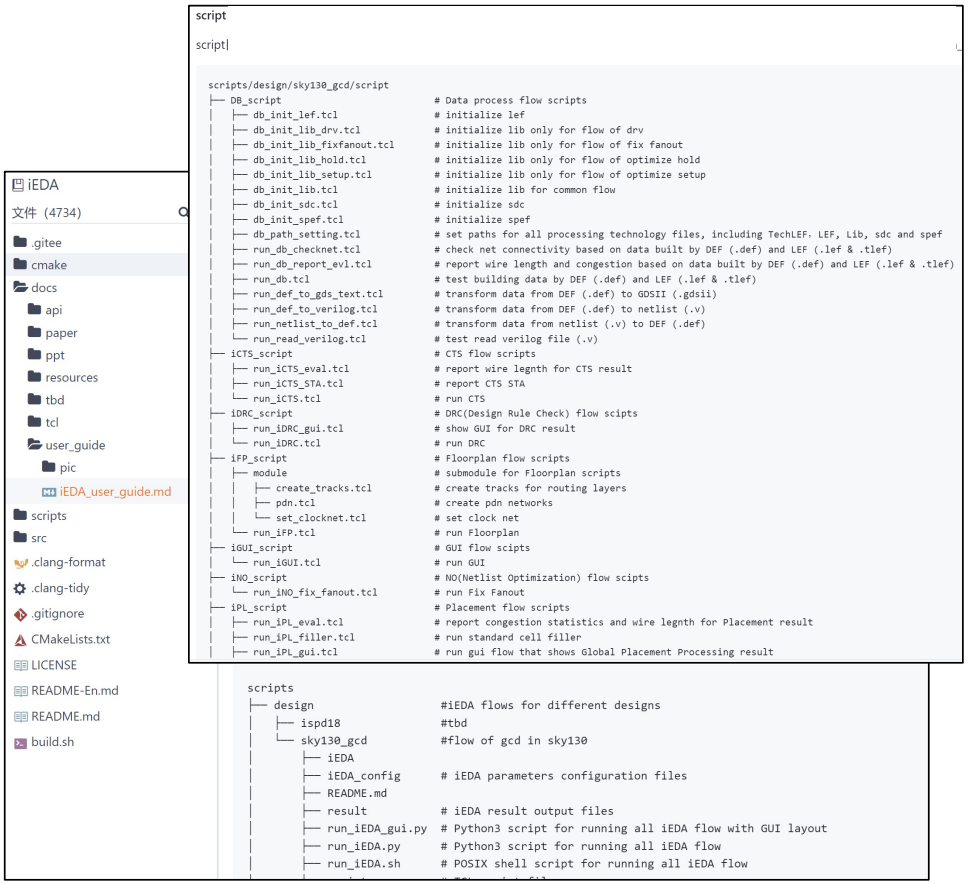
API list

API Command	Type	Description
set_num_threads	builder	set the numbers of threads
set_design_work_space	builder	set the directory to output the timing reports
readLiberty	builder	read the liberty files
readDesign	builder	read the design verilog file
readSpef	builder	read the spef file
readSdc	builder	read the sdc file
readAocv	builder	read the aocv files
makeOrFindRCTreeNode	builder	make RC tree internal node
makeOrFindRCTreeNode	builder	make RC tree pin node
incrCap	builder	set the node's cap
makeResistor	builder	make resistor edge of RC tree
updateRCTreeInfo	builder	update the RC info after making the RC tree

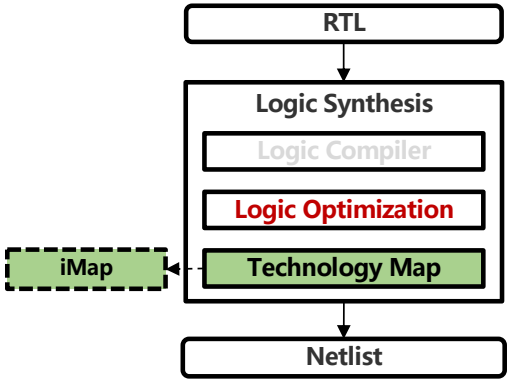
buildRCTree		
initRcTree		
initRcTree		
resetRcTree		
buildGraph		
isBuildGraph		
resetGraph		
resetGraphData		
insertBuffer		
removeBuffer		
repowerInstance		
moveInstance		
writeVerilog		
setSignificantDigits	builder	set the significant digits of the timing report
incrUpdateTiming	action	incremental propagation to update the timing data
updateTiming	action	update the timing data

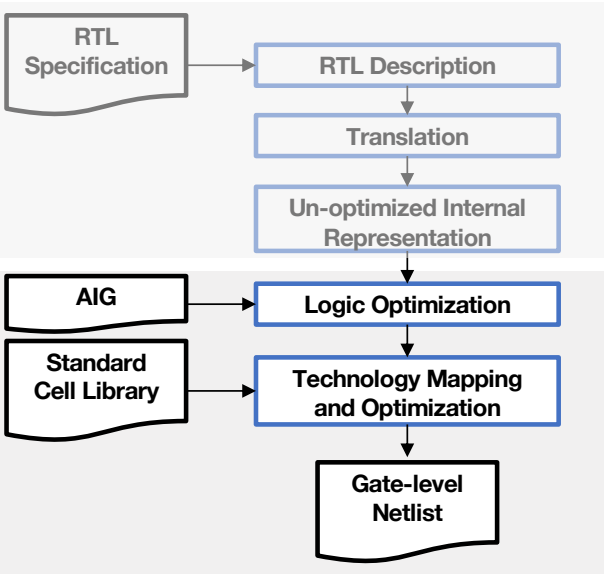
Doc Link：https://gitee.com/ieda-ipd/iEDA/tree/master/docs

User Manual

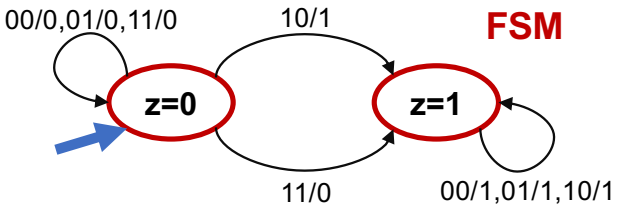


iEDA-Tool: iMAP (Tech Mapping)

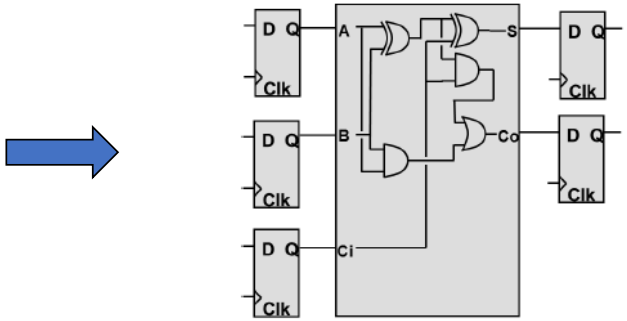




- ✓ iMAP 1.0 has completed the basic process mapping algorithm and logic optimization operators.
- ✓ The currently completed features include:
  - ✓ Data format support: AIG->Verilog
  - ✓ Logic synthesis operators: Rewrite, refactor, balance, LUT-opt, Map

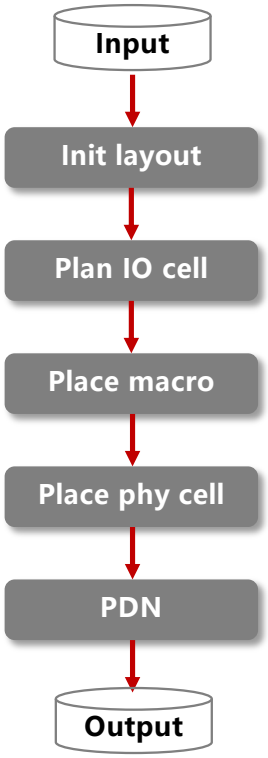


$$z(t) = c(t)d'(t) + c'(t)z(t-1)$$

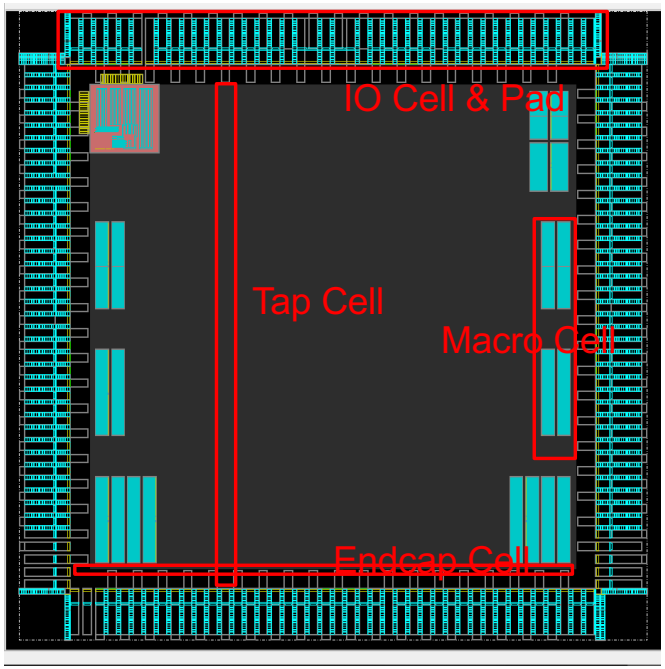


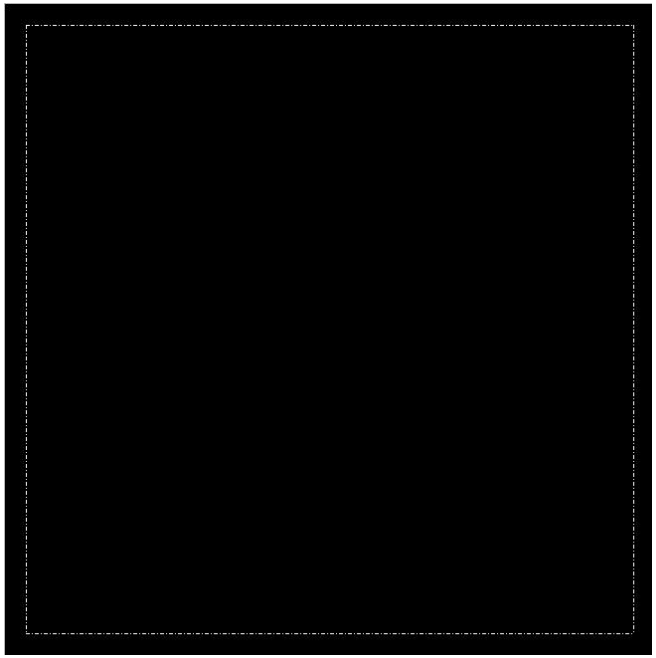
iEDA-Tool：iFP (Floorplan) and iPDN

Flow



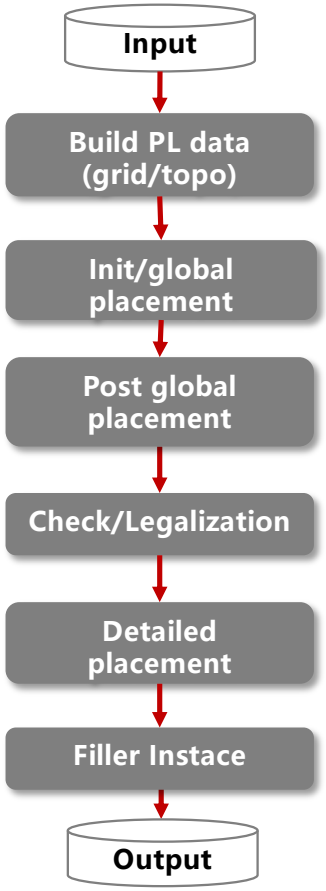
Key Metrics	Data
DIE Area	1.5 × 1.5 mm^2
DIE Utili	0.166554
Core Area	1.16 × 1.15 cm^2
Core Utili	0.279541
#IO Pin	110
#Instance	297504
#Net	311869
Pin	**pin (>= 32) = 2893**
PDN	M1、M2、M7、M8、M9、AP

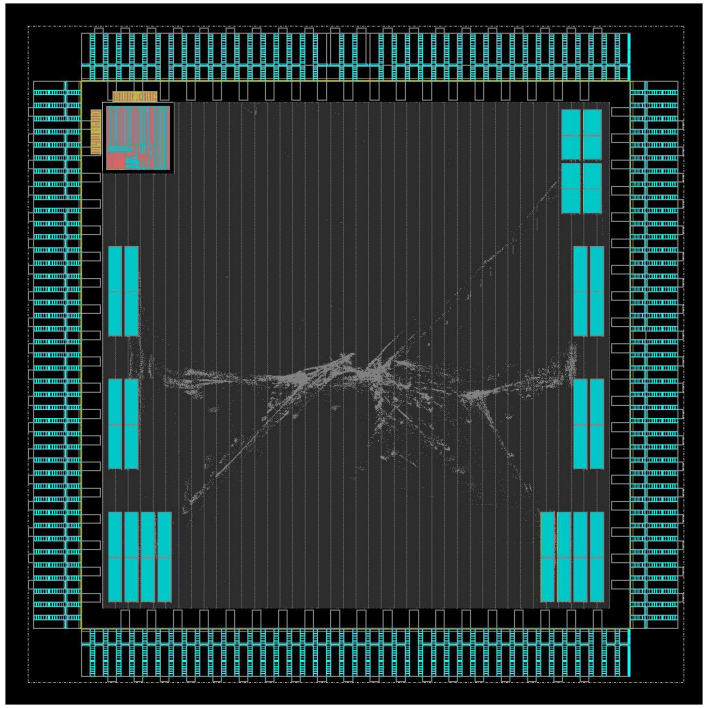




iEDA-Tool: iPL (Placement)

Flow





■ Min Wirelength Model

$$\min_{\boldsymbol{v}} \quad W(\boldsymbol{v})$$
$$s.t. \quad \rho_b(\boldsymbol{v}) \le \rho_0, \qquad \forall b \in B$$

where v is cell location, $W(\boldsymbol{v})$ is wirelength, $\rho_b(\boldsymbol{v})$ is the area density in $b \in B$, ρ_0 is density thredhold.

$$\boldsymbol{W(v)} \begin{cases} HPWL_{ex}(\mathbf{v}) = \max\limits_{i,j\in e} |x_i - x_j| \\ LSE_{ex} = \gamma\left(\ln\left(\sum\limits_{i\in e}\exp\left(\frac{x_i}{\gamma}\right)\right) + \ln\left(\sum\limits_{i\in e}\exp\left(\frac{-x_i}{\gamma}\right)\right)\right) \end{cases}$$

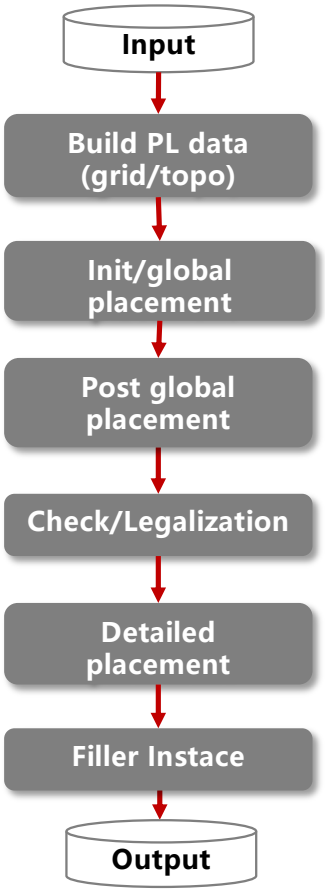
$$\boldsymbol{\rho_b(v)} \begin{cases} D(\boldsymbol{v}) = \frac{1}{2}\sum\limits_{v\in V} D_i(x,y) = \frac{1}{2}\sum\limits_{v\in V} q_i\psi_i(x,y) \\ \begin{cases} \nabla\cdot\nabla\psi(x,y) = -\rho(x,y), \\ \hat{\boldsymbol{n}}\cdot\psi(x,y) = \mathbf{0}, \qquad (x,y)\in\partial R \\ \iint_R \rho(x,y) = \iint_R \psi(x,y) = 0. \end{cases} \end{cases}$$

$$\min_{\boldsymbol{v}} \quad f(v) = W(\boldsymbol{v}) + \lambda \sum_{\forall b\in B} \boldsymbol{\rho_b}(\boldsymbol{v})$$

- **Nesterov Method or** Conjugate Gradient

iEDA-Tool: iPL (Placement)

Flow



Key parameter config	
Input	iFP.def, iFP.v
output	iPL_result.def, iPL.v
is_max_length_opt	Whether to enable max wirelength optimization
max_length_constraint	set max wirelength constraint
is_timing_aware_mode	Whether to enable timing opt
ignore_net_degree	ignore net whose pin number > k
num_threads	set number of CPU thread
[BUFFER] max_buffer_num	Set the number of using max buffer
[BUFFER] buffer_type	Set available buffer name
[GP-Wirelength] min_wirelength_force_bar	Control wirelength range
[GP-Density] target_density	Set target density
[GP-Density] bin_cnt_x	Set the number of horizontal Bin
[GP-Density] bin_cnt_y	Set the number of vertical Bin
[LG] global_right_padding	Set instance spacing (/site)
[DP] global_right_padding	Set instance spacing (/site)
[Filler] min_filler_width	Set min width of filler (/site)

Basic Summary

summary_report.txt

scripts > sky130 > result > pl > report > summary_report.txt

```
Generate the report at 2023-08-15T15:10:33
+-----------------------+----------+
| Base Info             | Value    |
+-----------------------+----------+
| Design                | gcd      |
| Utilization           | 0.098599 |
| Site Num              | 78 * 542 |
| Instances Count       | 795      |
| - Macro Count         | 0        |
| - StdCell Count       | 795      |
| -- FlipFlop Count     | 34       |
| -- Clock Buffer Count | 0        |
| -- Normal Logic Count | 761      |
| Nets Count            | 675      |
| - Signal Net Count    | 674      |
| - Clock Net Count     | 1        |
| - Reset Net Count     | 0        |
| - Other Net Count     | 0        |
+-----------------------+----------+

+-----------------------------------+------+
| Violation Info                    | Value |
+-----------------------------------+------+
| Core Range Violated Count         | 0    |
| Row/Site Alignment Violated Count | 0    |
| Power Alignment Violated Count    | 0    |
| Overlap Violated Count            | 0    |
+-----------------------------------+------+

+-----------------------------------+----------+
| Wirelength Info                   | Value    |
+-----------------------------------+----------+
| Total HPWL                        | 14402289 |
| Max HPWL                          | 328905   |
| Total STWL                        | 15057480 |
| Max STWL                          | 512025   |
| LongNet HPWL (Exceed 1000000) Count | 0      |
+-----------------------------------+----------+

+------------------+----------+
| Bin Density Info | Value    |
+------------------+----------+
| Peak BinDensity  | 1.000000 |
+------------------+----------+

+------------------+-----------+-----------+-----------+-----------+
| Clock Timing Info | Early WNS | Early TNS | Late WNS  | Late TNS  |
+------------------+-----------+-----------+-----------+-----------+
| core_clock        | 0.000000  | 0.000000  | -0.194720 | -2.818471 |
+------------------+-----------+-----------+-----------+-----------+

+----------------------------+-----------+
| Congestion Info            |           |
+----------------------------+-----------+
| Average Congestion of Edges | 0.537355 |
| Total Overflow             | 53.000000 |
| Maximal Overflow           | 18.000000 |
+----------------------------+-----------+
```

Wirelength
wl_detail_report.txt

Instance density

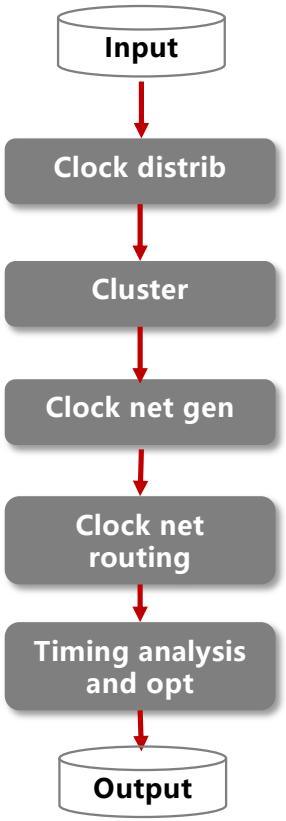
Timing

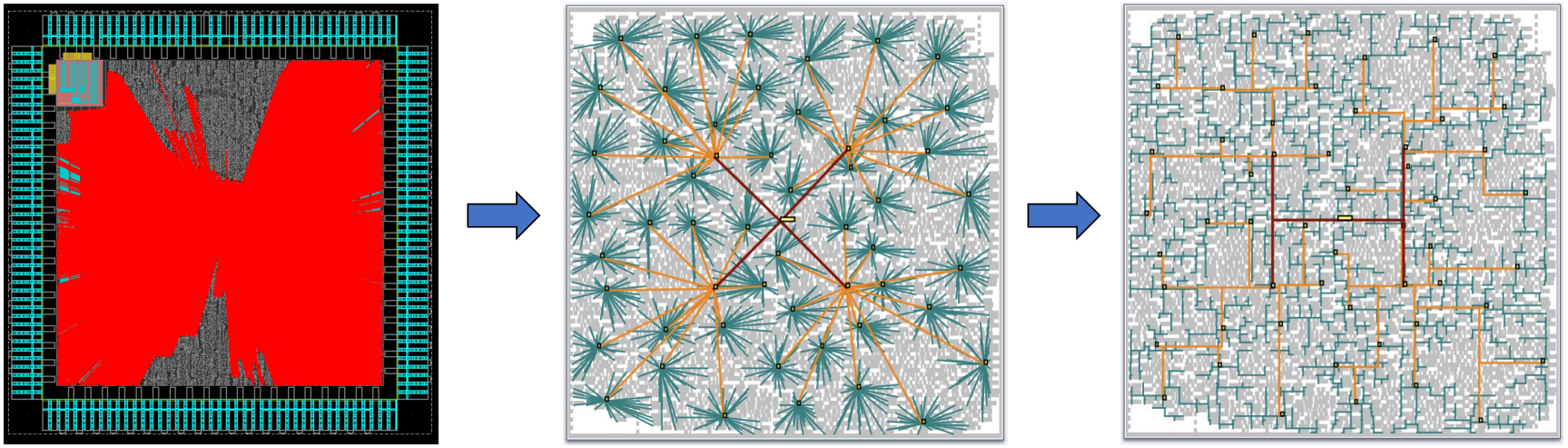
Congestion

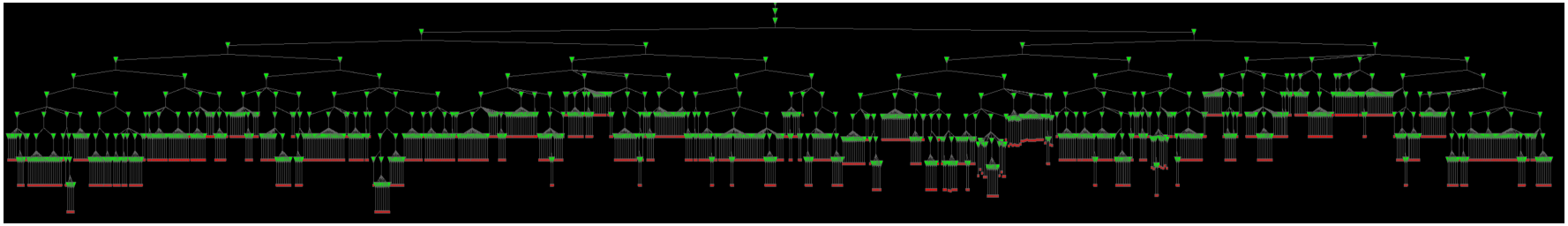
Design rule violation
violation_detail_report.txt

iEDA-Tool: iCTS (Clock Tree Synthesis)

Flow

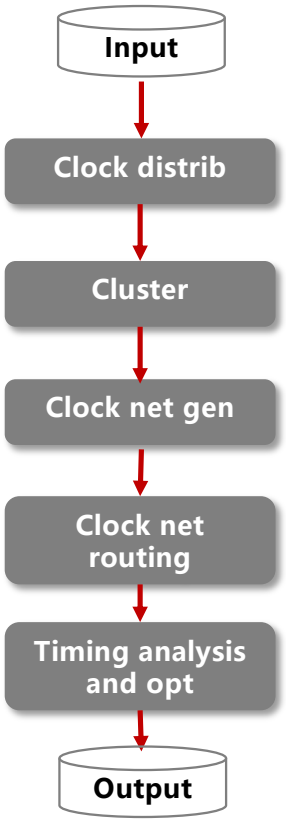






iEDA-Tool: iCTS (Clock Tree Synthesis)

Flow



Timing

- Latency (max delay)
- Skew

Level	Inst Num	Min Skew	Max Skew	Avg Skew	Violation
1	1210	6.62388e-05	0.0145301	0.00105275	0
2	204	0.000406356	0.0278176	0.00972537	0
3	80	0.0042316	0.0411625	0.0190886	0
4	41	0.00690457	0.0566811	0.0323446	0
5	22	0.0261657	0.0760005	0.0524973	0
6	13	0.0261657	0.0799602	0.0623044	0
7	7	0.0261657	0.08	0.0669329	0
8	4	0.0603809	0.08	0.0743834	0
9	2	0.0799208	0.08	0.0799604	0
10	1	0.08	0.08	0.08	0

Level	Inst Num	Min Delay	Max Delay	Avg Delay	Violation
1	1210	0.000237424	0.0432362	0.00143337	None
2	204	0.0518461	0.0983796	0.0688073	None
3	80	0.119261	0.174637	0.145464	None
4	41	0.187633	0.255905	0.219663	None
5	22	0.250207	0.319777	0.294133	None
6	13	0.324988	0.400232	0.365337	None
7	7	0.405067	0.452041	0.435055	None
8	4	0.500763	0.549897	0.522962	None
9	2	0.573994	0.578742	0.576368	None
10	1	0.608399	0.608399	0.608399	None

Power

- Buffering
- Wirelength

Type	Wire Length
Top	161.021
Trunk	2255.200
Leaf	9267.600
Total	11683.821
Max net length	232.360

Type	HP Wire Length
Top	161.021
Trunk	1347.840
Leaf	3871.380
Total	5380.241
Max net length	161.021

Name	Type	Inst Count	Inst Area (um^2)
CKBD12BWP35P140	Buffer	45	96.39
CKBD16BWP35P140	Buffer	8	22.176
CKBD20BWP35P140	Buffer	12	40.824
CKBD24BWP35P140	Buffer	63	254.016
CKBD4BWP35P140	Buffer	1082	954.324
CKBD6BWP35P140	Buffer	1129	1280.29
CKBD8BWP35P140	Buffer	81	122.472

Violation

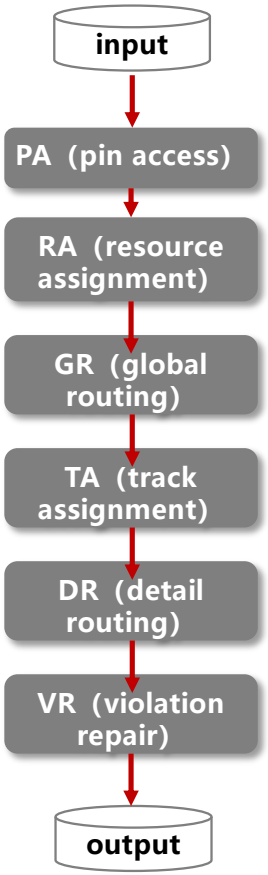
- Fanout
- Capacitance
- Slew (transition)

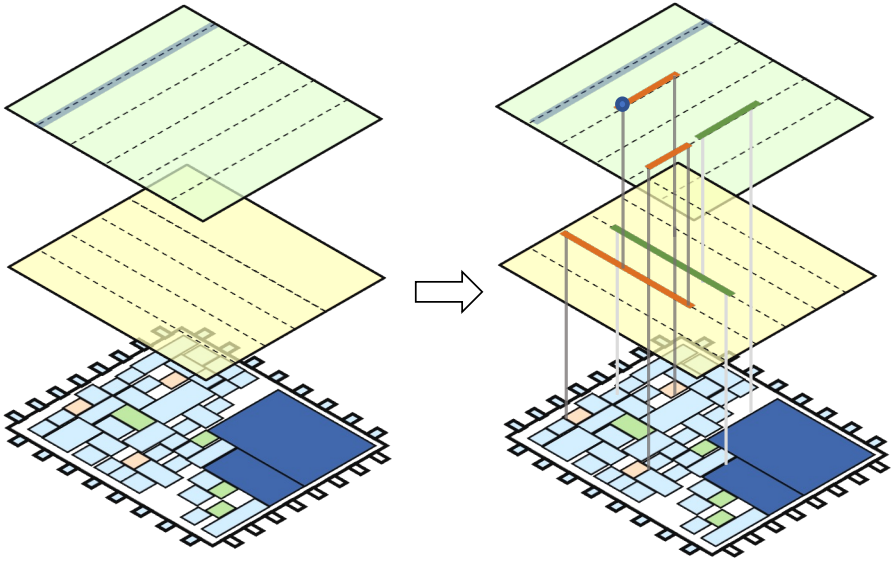
Level	Inst Num	Min Slew	Max Slew	Avg Slew	Violation
1	1210	0.0355823	0.0881141	0.0564704	970
2	204	0.0342527	0.0938317	0.0559007	134
3	80	0.0148774	0.103097	0.0581444	45
4	41	0.00736284	0.102664	0.0516092	20
5	22	0.0175251	0.103516	0.0535373	9
6	13	0.0116574	0.0884235	0.0402797	4
7	7	0.00706415	0.101609	0.0506611	3
8	4	0.015983	0.0220045	0.0188449	0
9	2	0.0259563	0.0286678	0.027312	0
10	1	0	2.22507e-308	0	0

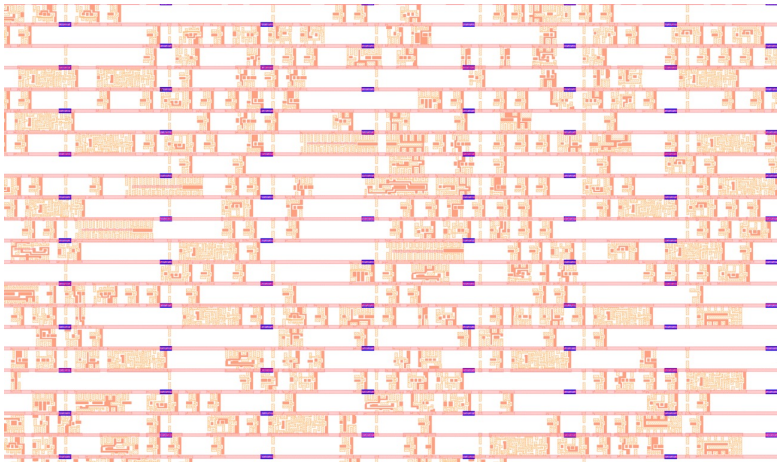
Net / InstPin	MaxTranTime	TranTime	TranSlack	CellPort	Remark
sdram_clk_o					
sdram_clk_o_15397_buf:I	0.800r/0.800f	1.583r/1.494f	-0.783r/-0.694f	CKBD24BWP35P140/I	R
sdram_clk_o					
u0_soc_top/u0_sdram_axi/u_core/U300:ZN	0.800r/0.800f	1.537r/1.446f	-0.737r/-0.646f	INVD1BWP40P140LVT/ZN	R
osc_25m_out_pad					
u0_clk:XOUT	5.000r/5.000f	5.704r/9.550f	-0.704r/-4.550f	PDXOEDG_V_G/XOUT	R
osc_100m_out_pad					
ul_clk:XOUT	5.000r/5.000f	5.704r/9.550f	-0.704r/-4.550f	PDXOEDG_V_G/XOUT	R
clk_hs_peri					
clk_hs_peri_11489_buf:I	0.800r/0.800f	0.850r/0.880f	-0.050r/-0.080f	CKBD24BWP35P140/I	R
u0_rcg/u0_pll_clk					
u0_rcg/ul_lvt_ckmux2hdv4:I1	0.267r/0.267f	0.189r/0.188f	0.078r/0.078f	CKMUX2D4BWP40P140LVT/I1	
u0_rcg/u0_pll_clk					
u0_rcg/u0_pll:FOUTPOSTDIV	0.267r/0.267f	0.000r/0.000f	0.267r/0.267f	PLLTS28HPMLAINT/FOUTPOSTDIV	
clk_core					
clk_core_1724_buf:I	0.800r/0.800f	0.522r/0.533f	0.278r/0.267f	CKBD4BWP35P140/I	
clk_hs_peri					
u0_soc_top/u0_sdram_axi/u_core/U300:I	0.800r/0.800f	0.519r/0.568f	0.281r/0.232f	INVD1BWP40P140LVT/I	
u0_soc_top/n495					
fanout_buf_40:I	0.437r/0.437f	0.098r/0.056f	0.339r/0.381f	BUFFD8BWP30P140LVT/I	

iEDA-Tool: iRT (Routing)

Flow



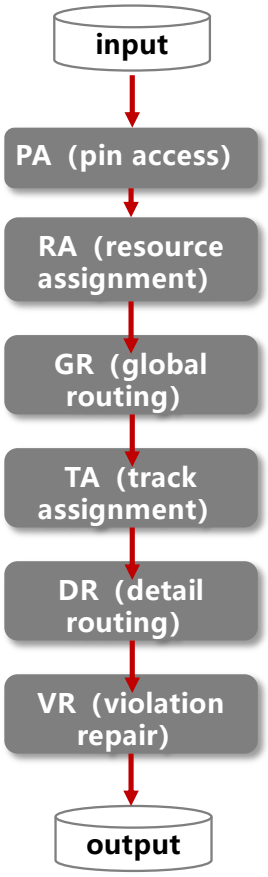




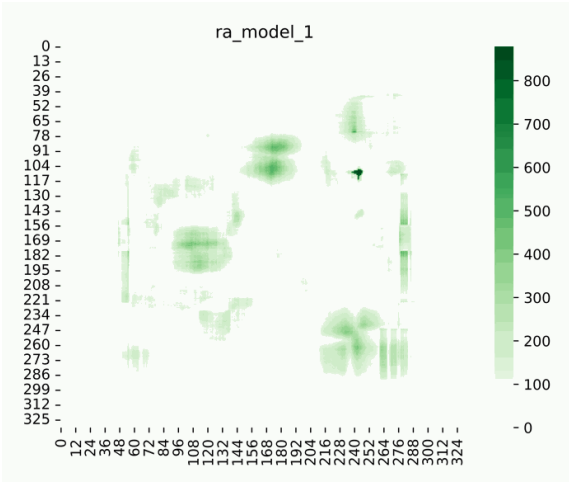
- **Optimization metrics:** wirelength, timing, congestion, DRC
- **Optimization operations:** Global routing: Track allocation: Detailed routing
- **Routing algorithms:** Pattern routing, A* routing, Steiner tree, Non-linear programming, Integer programming

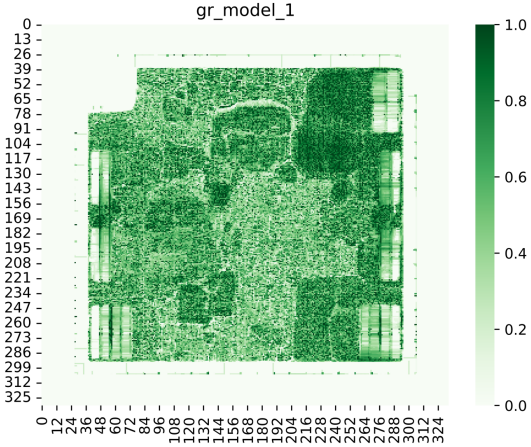
iEDA-Tool: iRT (Routing)

Flow



Layout resource/congestion





Design rule check

Drc Summary

DRC Type	Number
Cut Different Layer Spacing	433141
Cut EOL Spacing	197803
Cut Enclosure	152168
Cut EnclosureEdge	0
Cut Spacing	358281
Metal Corner Filling Spacing	10443
Metal EOL Spacing	869415
Metal JogToJog Spacing	0
Metal Notch Spacing	733497
Metal Parallel Run Length Spacing	864355
Metal Short	1745445
MinHole	1260
MinStep	670823
Minimal Area	1248072

Pin Access

Access Type	Pin Number
Track Grid	876856(75.2479%)
On Track	259825(22.297%)
On Shape	28608(2.45501%)
Total	1165289

Routing Layer	Port Number	Access Point Number
M1	806086(68.3279%)	799044(68.5705%)
M2	366214(31.0422%)	362248(31.0865%)
M3	7073(0.599543%)	3997(0.343005%)
M4	358(0.0303459%)	0(0%)
M5	0(0%)	0(0%)
M6	0(0%)	0(0%)
M7	0(0%)	0(0%)
M8	0(0%)	0(0%)
M9	0(0%)	0(0%)
AP	0(0%)	0(0%)
Total	1179731	1165289

Wirelength and via

Routing Layer	Wire Length / um
M1	9774(0.117785%)
M2	846292(10.1985%)
M3	1.98405e+06(23.9095%)
M4	1.78748e+06(21.5406%)
M5	1.29642e+06(15.6229%)
M6	1.41202e+06(17.016%)
M7	960890(11.5795%)
M8	539.92(0.00650648%)
M9	720(0.00867659%)
AP	0(0%)
Total	8.29819e+06

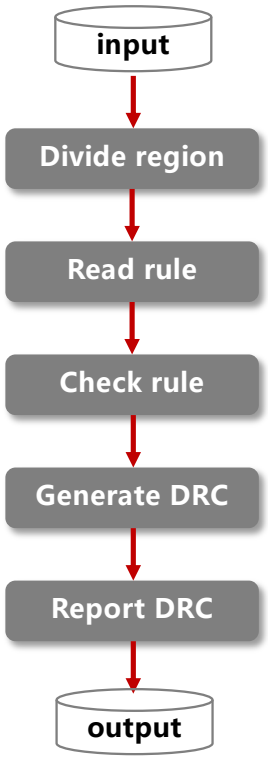
Cut Layer	Via Number
CO	0(0%)
VIA1	595417(30.6475%)
VIA2	682833(35.147%)
VIA3	400386(20.6088%)
VIA4	135600(6.97965%)
VIA5	89437(4.60353%)
VIA6	38709(1.99244%)
VIA7	262(0.0134857%)
VIA8	148(0.0076179%)
RV	0(0%)
Total	1942792

Resource Overflow	GCell Number
[0,0.1)	921387(83.1%)
[0.1,0.2)	57544(5.19%)
[0.2,0.3)	51492(4.64%)
[0.3,0.4)	40084(3.61%)
[0.4,0.5)	21944(1.98%)
[0.5,0.6)	10780(0.972%)
[0.6,0.7)	4140(0.373%)
[0.7,0.8)	1223(0.11%)
[0.8,0.9)	222(0.02%)
[0.9,1]	74(0.00667%)
Total	1108890

Access Overflow	GCell Number
[0,0.1)	1.78338e+06(80.4%)
[0.1,0.2)	108739(4.9%)
[0.2,0.3)	79939(3.6%)
[0.3,0.4)	90020(4.06%)
[0.4,0.5)	56112(2.53%)
[0.5,0.6)	36741(1.66%)
[0.6,0.7)	30046(1.35%)
[0.7,0.8)	12155(0.548%)
[0.8,0.9)	8771(0.395%)
[0.9,1]	11881(0.536%)
Total	2217780

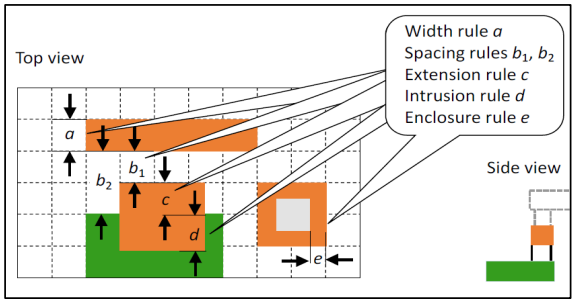
iEDA-Tool: iDRC (Design Rule Check)

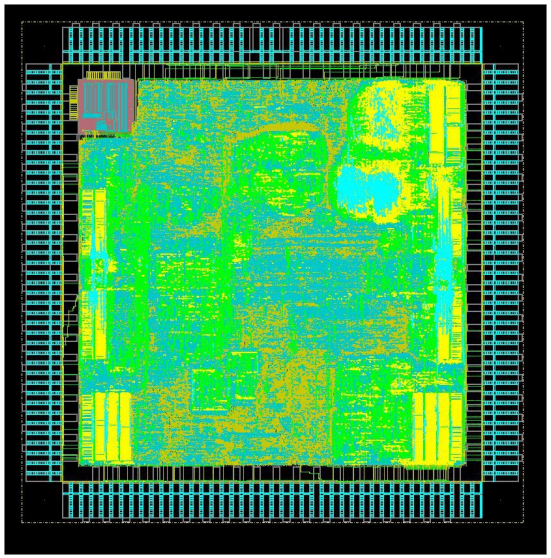
Flow

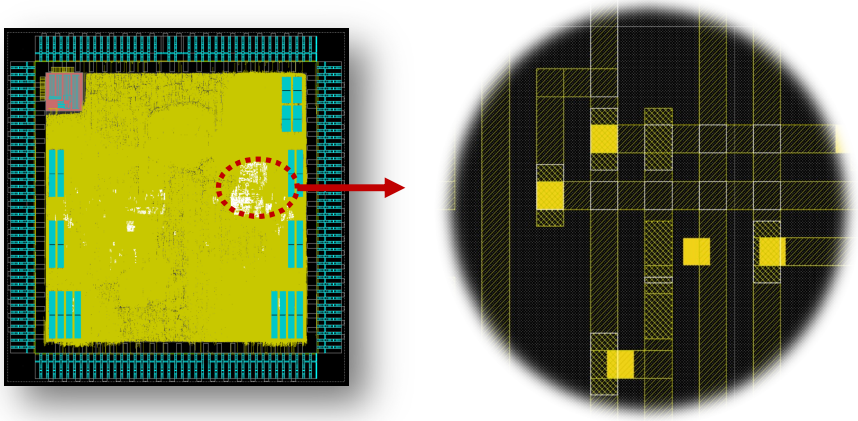


Support DRC Rules:

- **Cut Different Layer Spacing**
- **Cut EOL Spacing**
- **Cut Enclosure**
- **Cut EnclosureEdge**
- **Cut Spacing**
- **Metal Corner Filling Spacing**
- **Metal EOL Spacing**
- **Metal JogToJog Spacing**
- **Metal Notch Spacing**
- **Metal Parallel Run Length Spacing**
- **Metal Short**
- **MinHole**
- **MinStep**
- **Minimal Area**



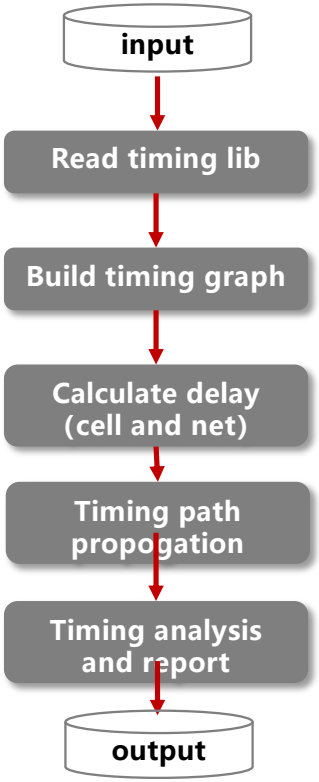


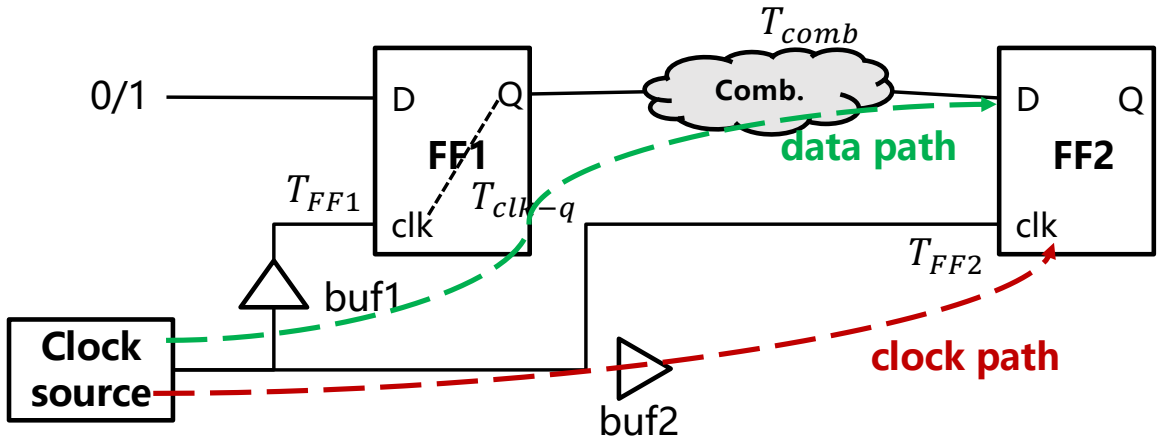


DRC Visulization

iEDA-Tool: iSTA (Static Timing Analysis)

FLow



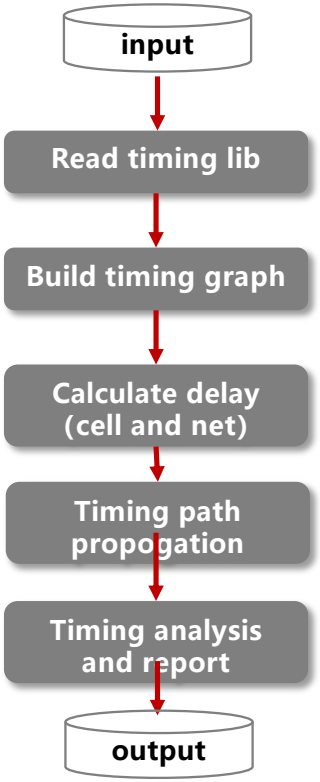


$$T_{FF1} + T_{clk-q} + T_{comb} + T_{setup} - T_{FF2} - T = T_{slack}^{late} \geq 0$$ **Setup Constraint**

$$T_{FF1} + T_{clk-q} + T_{comb} - T_{hold} - T_{FF2} = T_{slack}^{early} \geq 0$$ **Hold Constraint**

iEDA-Tool: iSTA (Static Timing Analysis)

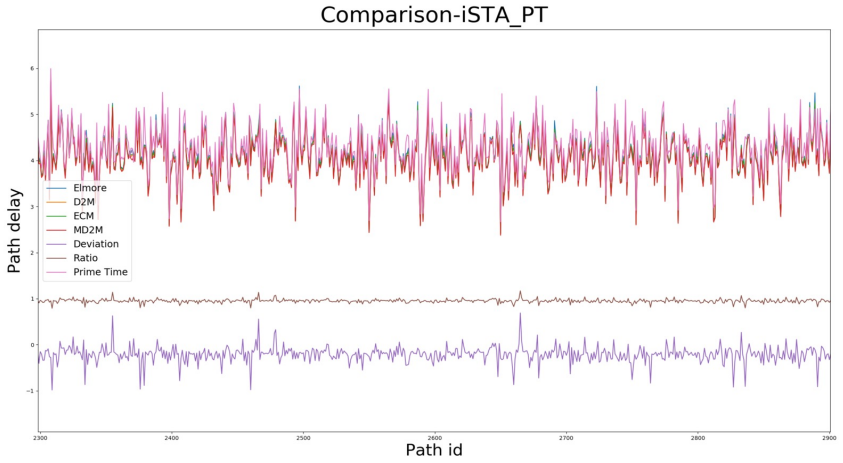
FLow



Feature

Feature
Support hierarchy netlist and def
Basic setup/hold analysis
Support NLDM/Elmore
Support CCS model
Support high-level net delay model
Support sdf mark
OCV
AOCV
POCV
Consider IRDrop analysis on multi-voltage domain
Hierarchy analysis
Crosstalk analysis
clock gate analysis
Latch analysis

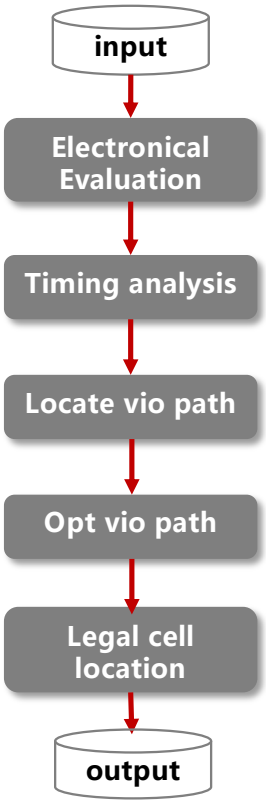
Point	Fanout	Capacitance	Resistance	Transition	Delta Delay	Derate	Incr	Path
u1_clk:XC (PDXOEDG_V_G)		0.002	0.000	0.000		1.000	0.000	0.000r
sys_clk_100m (clock net)	1				0.000			
u1_clk_xc_donottouch:I (CKBD12BWP40P140LVT)		0.002	0.000	0.000		1.000	0.000	0.000r
u1_clk_xc_donottouch:Z (CKBD12BWP40P140LVT)		0.002	0.000	0.006		0.885	0.011	0.011r
sys_clk_100m_buf (clock net)	2				0.000			
u0_rcg/u1_lvt_ckmux2hdv4:I0 (CKMUX2D4BWP40P140LVT)		0.001	0.000	0.006		1.000	0.000	0.011r
u0_rcg/u1_lvt_ckmux2hdv4:Z (CKMUX2D4BWP40P140LVT)		0.006	0.000	0.018		0.885	0.032	0.043r
u0_rcg/mux_core_clk (clock net)	5				0.000			
u0_rcg/mux_core_clk_0_buf:I (CKBD4BWP35P140)		0.001	0.000	0.018		1.000	0.000	0.043r
u0_rcg/mux_core_clk_0_buf:Z (CKBD4BWP35P140)		0.008	0.000	0.015		0.885	0.021	0.064r
u0_rcg/mux_core_clk_0 (clock net)	17				0.000			
u0_rcg/mux_core_clk_div3/gt_en1_reg:CP (DFSNQD1BWP40P140LVT)		0.000	0.000	0.015		1.000	0.000	0.064r
clock CLK_u1_clk_XC (rise edge)							0	0
clock network delay (propagated)							0.064	0.064
u0_rcg/mux_core_clk_div3/gt_en1_reg:CP (DFSNQD1BWP40P140LVT)		0.000	0.000	0.015		1.000	0.000	0.064r
u0_rcg/mux_core_clk_div3/gt_en1_reg:Q (DFSNQD1BWP40P140LVT)		0.001	0.000	0.009		0.820	0.045	0.109r
u0_rcg/mux_core_clk_div3/gt_en1 (net)	1				0.000			
u0_rcg/mux_core_clk_div3/U_GT1:E (CKLNQD4BWP40P140LVT)		0.001	0.000	0.009		1.000	0.000	0.109r
u1_clk:XC (PDXOEDG_V_G)		0.002	0.000	0.000		1.000	0.000	0.000r
sys_clk_100m (clock net)	1				0.000			
u1_clk_xc_donottouch:I (CKBD12BWP40P140LVT)		0.002	0.000	0.000		1.000	0.000	0.000r
u1_clk_xc_donottouch:Z (CKBD12BWP40P140LVT)		0.002	0.000	0.006		1.039	0.013	0.013r
sys_clk_100m_buf (clock net)	2				0.000			
u0_rcg/u1_lvt_ckmux2hdv4:I0 (CKMUX2D4BWP40P140LVT)		0.001	0.000	0.006		1.000	0.000	0.013r
u0_rcg/u1_lvt_ckmux2hdv4:Z (CKMUX2D4BWP40P140LVT)		0.006	0.000	0.018		1.039	0.038	0.051r
u0_rcg/mux_core_clk (clock net)	5				0.000			
u0_rcg/mux_core_clk_0_buf:I (CKBD4BWP35P140)		0.001	0.000	0.018		1.000	0.000	0.051r
u0_rcg/mux_core_clk_0_buf:Z (CKBD4BWP35P140)		0.008	0.000	0.015		1.039	0.025	0.076r
u0_rcg/mux_core_clk_0 (clock net)	17				NA			
u0_rcg/mux_core_clk_div3/U_GT1:CP (CKLNQD4BWP40P140LVT)		0.001	0.000	0.000		1.000	0.000	0.076r
clock CLK_u1_clk_XC (rise edge)							0	0
clock network delay (propagated)							0.076	0.076
u0_rcg/mux_core_clk_div3/U_GT1:CP (CKLNQD4BWP40P140LVT)								r
library hold time							0.000	0.076
clock reconvergence pessimism						-0.011	0.064	
data require time								0.064
data arrival time								0.109
slack (MET)								0.045



pt/ista ratio	value
mean	1.11
variance	0.00095
median	1.107
maximum	1.5404
minimum	0.9035

iEDA-Tool: iTO (Timing Optimization)

Flow



Key parameter config	
Input	iPL.def, iCTS.def
output	iTO_setup_result.def, iTO_hold_reslut.def
setup_slack_margin	setup slack value
hold_slack_margin	hold slack value
max_buffer_percent	Area ratio of inserted buffer
max_utilization	Core utilization
DRV_insert_buffers	Available buffer for optimizing DRV
setup_insert_buffers	Available buffer for optimizing setup
hold_insert_buffers	Available buffer for optimizing hold
number_passes_allowed_decreasing_slack	The number of times that WNS is allowed continuously decrease when opt setup
rebuffer_max_fanout	For setup, a wire network is not optimized for buffer insertion when its fanout exceeds this value
split_load_min_fanout	For setup, fanout is reduced by inserting a buffer when fanout is greater than this value

DRV report

```
path
Worst Slack: -5.88383
Found 3 slew violations.
Found 11 capacitance violations.
Found 0 fanout violations.
Found 0 long wires.
Before ViolationFix | slew_vio: 3 cap_vio: 11 fanout_vio: 0 length_vio: 0
The 1th check
After ViolationFix | slew_vio: 3 cap_vio: 0 fanout_vio: 0 length_vio: 0
The 2th check
After ViolationFix | slew_vio: 0 cap_vio: 0 fanout_vio: 0 length_vio: 0
DRV_net_3
Inserted 11 buffers in 12 nets.
Resized 0 instances.
```

Setup report

```
Inserted 10 hold buffers.

Worst Hold Path Launch : u0_soc_top/u0_sdram_axi/u_core/sample_data0_q_reg_8_:CP
Worst Hold Path Capture: u0_soc_top/u0_sdram_axi/u_core/sample_data_q_reg_8_:CP

The 1-th timing check.
    worst hold slack: -1.28225
Unable to repair all hold violations. There are still 16 endpoints with hold violation.
Max utilization reached.
```

Clock Group	Hold TNS	Hold WNS
CLK_chiplink_tx_clk	0	0
CLK_clk_hs_peri	-185.768	-1.27825
CLK_div2_core	-2606.7	-0.106129
CLK_div2_hs_peri	-216.759	-0.028571
CLK_div3_hs_peri	-72.5124	-0.028571
CLK_div4_core	-1304.1	-0.106129
CLK_div4_hs_peri	-185.768	-1.27825
CLK_div4_peri	-231.408	-0.042802
CLK_sdram_clk_o	0	0
CLK_spi_clk	0	0
CLK_spi_clk_out	0	0
CLK_u0_chiplink_rx_clk_pad_PAD	-89.8732	-0.028408
CLK_u0_clk_XC	-2987.42	-0.106129
CLK_u0_pll_FOUTPOSTDIV	-8546.64	-0.106129
CLK_u1_clk_XC	-2755.16	-0.106129

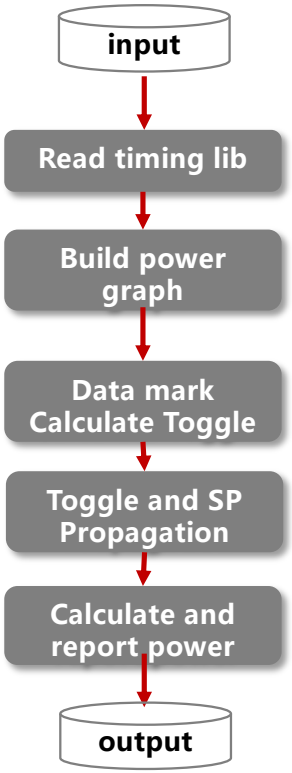
Clock Group	Hold TNS	Hold WNS
CLK_chiplink_tx_clk	0	0
CLK_clk_hs_peri	0	0
CLK_div2_core	0	0
CLK_div2_hs_peri	0	0
CLK_div3_hs_peri	0	0
CLK_div4_core	0	0
CLK_div4_hs_peri	0	0
CLK_div4_peri	0	0
CLK_sdram_clk_o	0	0
CLK_spi_clk	0	0
CLK_spi_clk_out	0	0
CLK_u0_chiplink_rx_clk_pad_PAD	0	0
CLK_u0_clk_XC	0	0
CLK_u0_pll_FOUTPOSTDIV	0	0
CLK_u1_clk_XC	0	0

Hold report

- Fix timing design rule violation
  - Max cap/Max slew/Max wirelength/Max fanout
- Fix hold time
- Fix setup time
- Cell sizing
- Buffer Insertion
- Load Insertion
- Buffer/load location

iEDA-Tool: iPW (Power Analysis)

Flow



API	Description
buildGraph	Build iPW graph data structure
readVCD	Parse the VCD file
buildSeqGraph	Build timing subgraph
checkPipelineLoop	Detect PipeLine loop
levelizeSeqGraph	Grade timing subgraph
propagateToggleSP	Propagate Toggle and SP data on the graph
calcLeakagePower	Calculate the leakage power
calcInternalPower	Calculate internal power
calcSwitchPower	Calculate switching power
analyzeGroupPower	Analyze power data
reportPower	Output power report

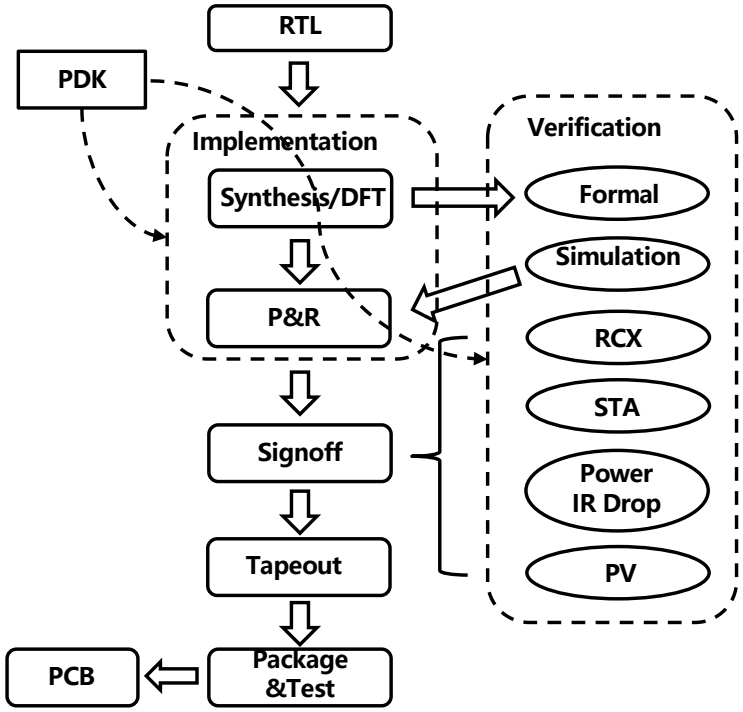
```
Generate the report at 2023-05-06T09:54:06
Report : Averaged Power
+--------------+--------------+--------------+--------------+-------------+-----------+
| Power Group  | Internal Power | Switch Power | Leakage Power | Total Power | (%)       |
+--------------+--------------+--------------+--------------+-------------+-----------+
| combinational | 1.064e-07    | 5.063e-09    | 3.079e-08    | 1.422e-07   | (27.595%) |
| sequential   | 2.862e-07    | 7.337e-09    | 7.963e-08    | 3.732e-07   | (72.405%) |
+--------------+--------------+--------------+--------------+-------------+-----------+
Net Switch Power  ==  1.240e-08 (2.406%)
Cell Internal Power  ==  3.926e-07 (76.173%)
Cell Leakage Power  ==  1.104e-07 (21.422%)
Total Power  ==  5.154e-07
```

```
I0506 09:50:50.732399 3182449 PwrPropagateConst.cc:166] propagate const start
I0506 09:50:50.732499 3182449 PwrPropagateConst.cc:270] propagate const end
I0506 09:50:50.732555 3182449 PwrPropagateConst.cc:272] propagate const memory usage 0MB
I0506 09:50:50.732573 3182449 PwrPropagateConst.cc:274] propagate const time elapsed 0.000176s
I0506 09:50:50.732645 3182449 PwrPropagateToggleSP.cc:186] propagate toggle sp start
I0506 09:50:50.736701 3182449 PwrPropagateToggleSP.cc:288] propagate toggle sp end
I0506 09:50:50.737669 3182449 PwrPropagateToggleSP.cc:291] propagate toggle sp memory usage 0MB
I0506 09:50:50.737720 3182449 PwrPropagateToggleSP.cc:293] propagate toggle sp time elapsed 0.005075s
I0506 09:50:50.737866 3182449 PwrPropagateClock.cc:53] propagate clock start
I0506 09:50:50.737897 3182449 PwrPropagateClock.cc:64] propagate clock end
I0506 09:50:50.737979 3182449 PwrPropagateClock.cc:66] propagate clock memory usage 0MB
I0506 09:50:50.738003 3182449 PwrPropagateClock.cc:68] propagate clock time elapsed 0.000138s
I0506 09:50:50.738090 3182449 PwrCalcLeakagePower.cc:54] calc leakage power start
```

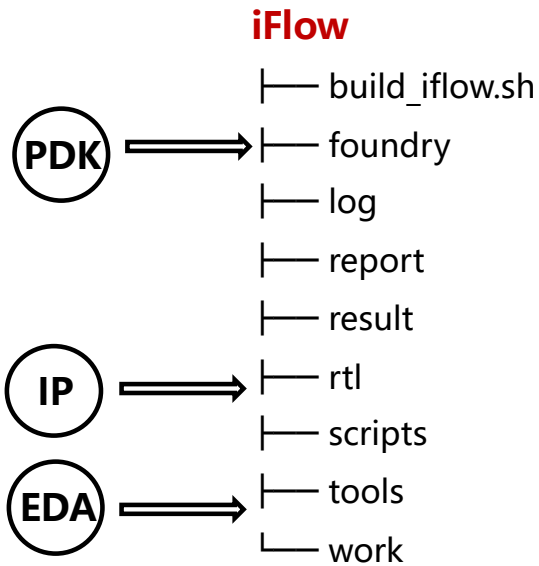
- Evaluate power before / during / after the physical design process
- Average model
- Timing window (coming soon)
- VCD parser
- Report/API

iFlow: A Chip Design Flow

- **iFlow: supporting different EDA tools, PDKs, designs**



Chip design flow

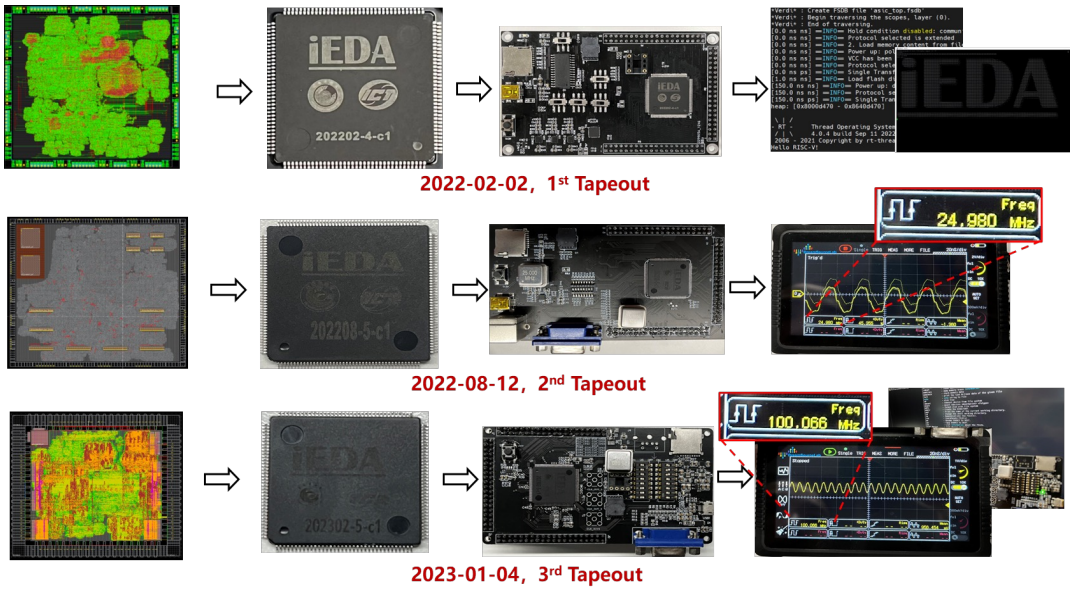


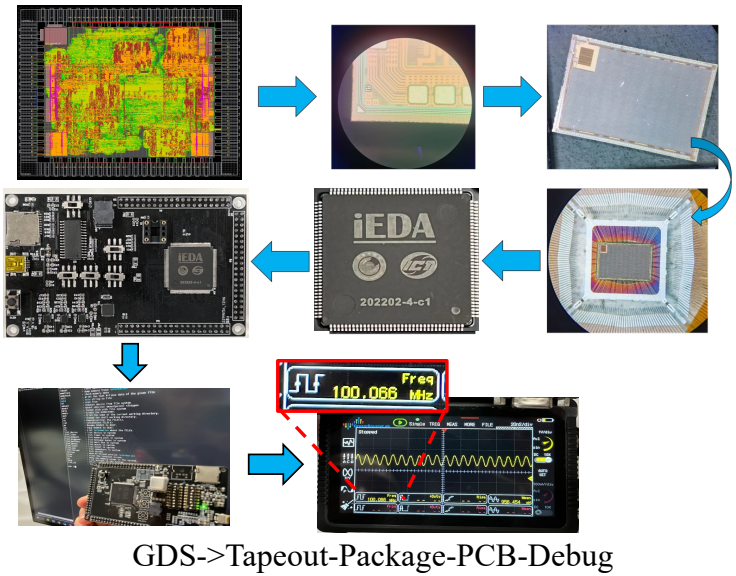
Introduction

iEDA

iEDA Application

iEDA-Tapeout





GDS->Tapeout-Package-PCB-Debug

1st Tapeout

- **RTL**：**ysyx(一生一芯)-03**
- **PDK**：110nm
- **Area**：**3mm × 3.5** mm
- **Power**：dynamic = 48mW，leakage = 7 mW
- **Freq.**：**25M**Hz
- **Scale**：>**70万** Gates
- **Features**：5 pipeline，Chiplink、UART、SPI，PCB clock，support RT-thread

2nd Tapeout

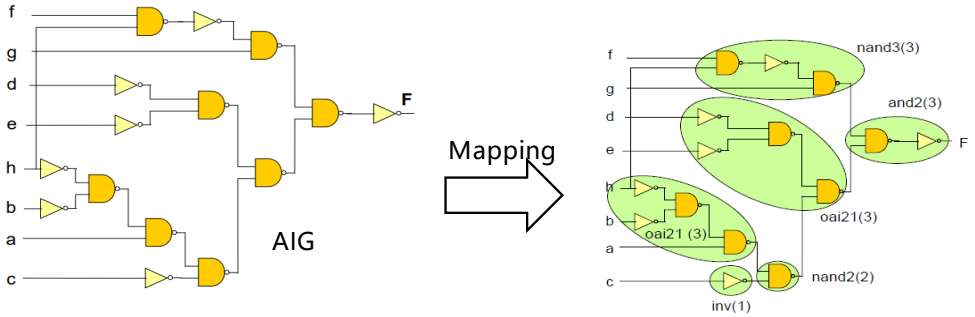
- **RTL**：**ysyx(一生一芯)-04**
- **PDK**：110nm
- **Area**：**4.5mm × 4.5** mm
- **Power**：dynamic = 343mW，leakage = **21** mW
- **Freq.**：**25M**Hz
- **Scale**：>**1.5M** Gates
- **Features**：11 pipelines with cache，IP：UART、VGA、PS/2、SPI、SDRAM、 2 PLLs，support Linux

3rd Tapeout

- **RTL**：**ysyx(一生一芯)-04**
- **PDK**：28nm
- **Area**：**1.5mm × 1.5** mm
- **Power**：dynamic = **317**mW，leakage = **29** mW
- **Freq.**：**200M**Hz
- **Scale**：>**1.5M** Gates
- **Features**：11 pipelines with cache，IP：UART、VGA、PS/2、SPI、SDRAM、 2 PLLs，support Linux

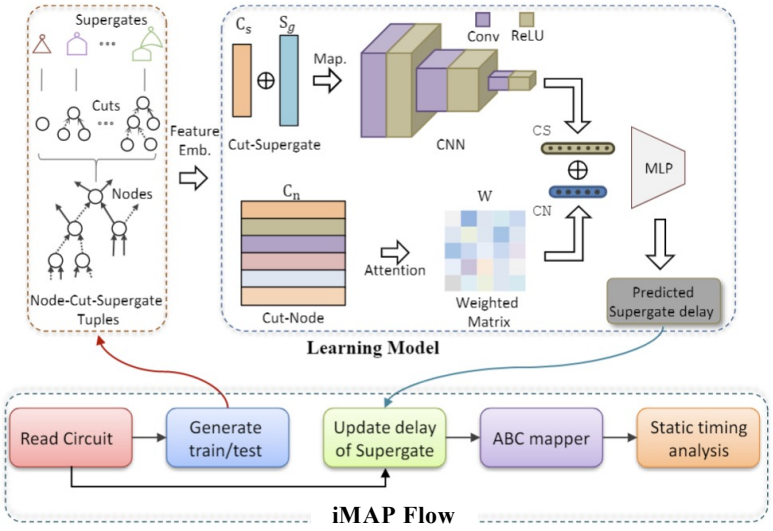
Research：Learning to Optimize Tech Mapping

- **Based on iMAP，we propose a ML method to predict cut delay**



Circuits	Estimated Results Area(μm²)	LI-Delay(ps)	Actual Results Area(μm²)	Delay(ps)	Δ Delay
adder	898.31	2,613.78	898.13	3,770.65	44%
bar	2,681.62	152.96	2,680.39	1,114.9	629%
log2	26,556.98	3,891.66	26,561.26	6,797.77	75%
cavlc	463.27	185.07	463.29	93.2	50%
int2float	158.61	174.27	158.63	91.7	47%
ctrl	106.92	98.53	106.84	89.9	9%

LI-Delay refers to the load-independent delay estimation in ABC [1]. The actual delay is computed by the non-linear delay model.



- AiMap: Learning to Improve Technology Mapping for ASICs via Delay Prediction, in Proc. of ICCD'23.

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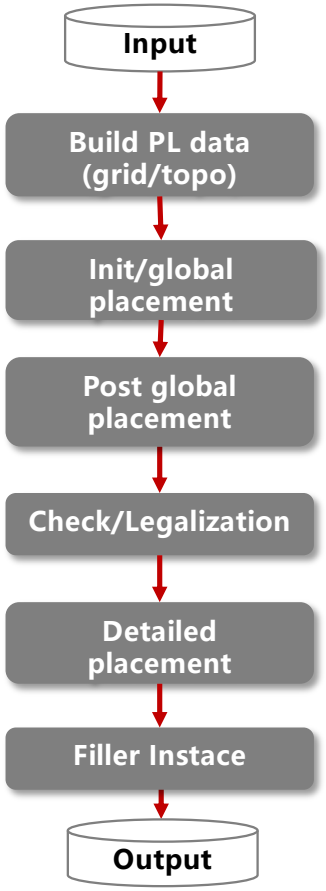
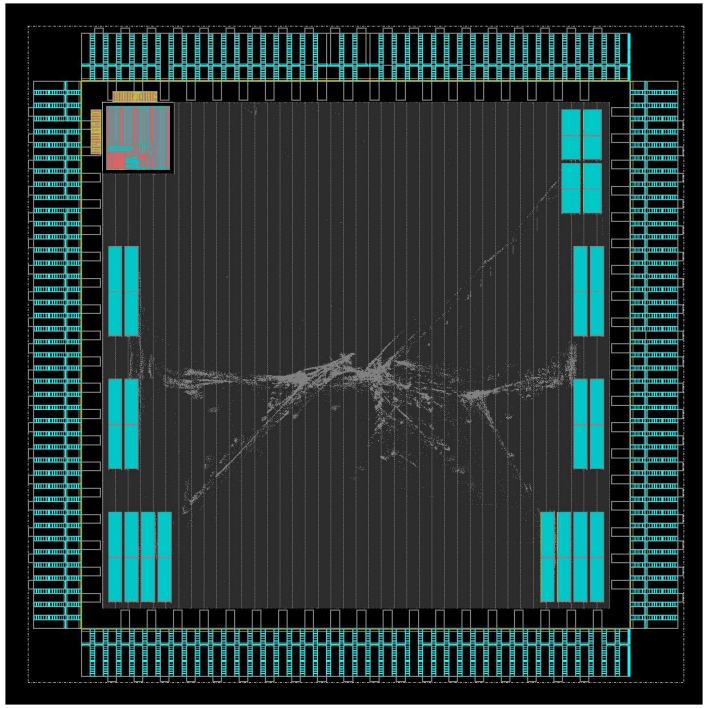
Flow





■ Min Wirelength Model

$$\min_{\boldsymbol{v}} \quad W(\boldsymbol{v})$$
$$s.t. \quad \rho_b(\boldsymbol{v}) \le \rho_0, \qquad \forall b \in B$$

where v is cell location, $W(\boldsymbol{v})$ is wirelength, $\rho_b(\boldsymbol{v})$ is the area density in $b \in B$, ρ_0 is density thredhold.

$$\boldsymbol{W(v)} \begin{cases} HPWL_{ex}(\mathbf{v}) = \max_{i,j\in e} |x_i - x_j| \\ LSE_{ex} = \gamma\left(\ln\left(\sum_{i\in e}\exp\left(\frac{x_i}{\gamma}\right)\right) + \ln\left(\sum_{i\in e}\exp\left(\frac{-x_i}{\gamma}\right)\right)\right) \end{cases}$$

$$\boldsymbol{\rho_b(v)} \begin{cases} D(\boldsymbol{v}) = \frac{1}{2}\sum_{v\in V} D_i(x,y) = \frac{1}{2}\sum_{v\in V} q_i\psi_i(x,y) \\ \begin{cases} \nabla\cdot\nabla\psi(x,y) = -\rho(x,y), \\ \hat{\boldsymbol{n}}\cdot\psi(x,y) = \mathbf{0}, \qquad (x,y)\in\partial R \\ \iint_R \rho(x,y) = \iint_R \psi(x,y) = 0. \end{cases} \end{cases}$$

$$\min_{\boldsymbol{v}} \quad f(v) = W(\boldsymbol{v}) + \lambda \sum_{\forall b\in B} \boldsymbol{\rho_b}(\boldsymbol{v})$$

- **Nesterov Method or Conjugate Gradient**

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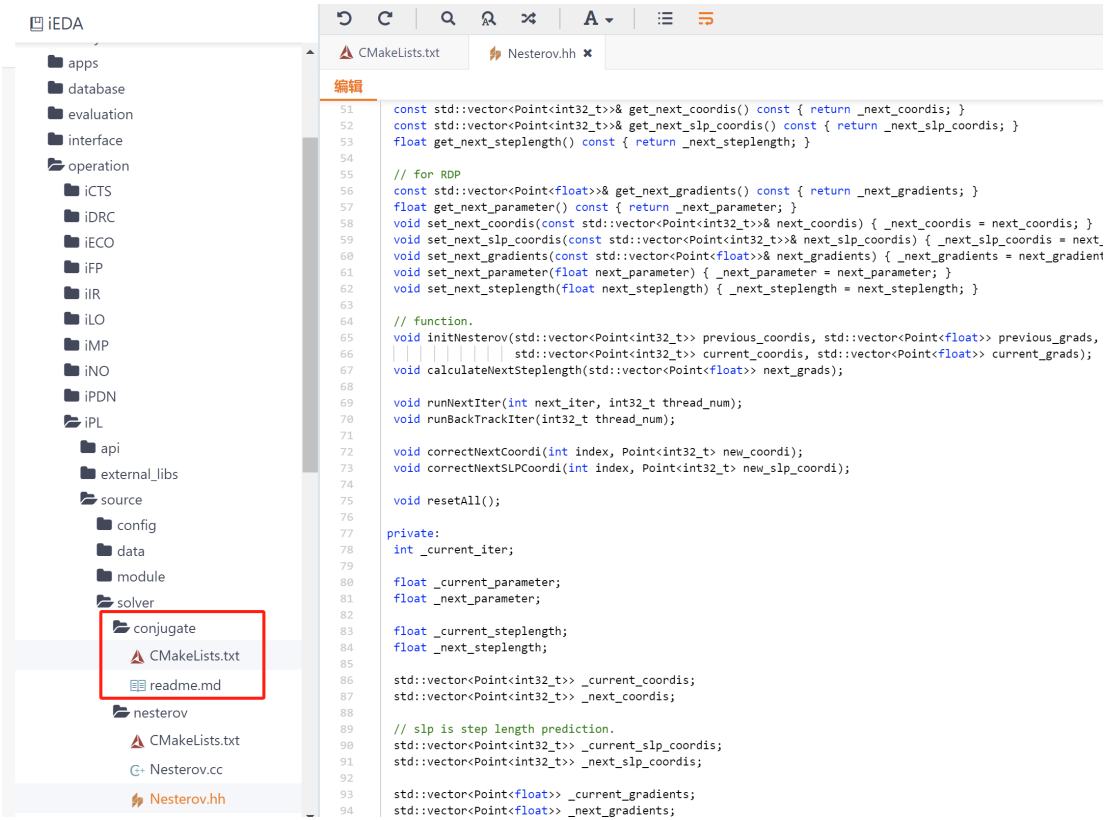
- With some linear algebra, the CG algorithm can be simplified as

1. Given x_0, $r_0 = Ax_0 - b$, $p_0 = -r_0$
2. For $k = 0,1,2,\ldots$ until $\|r_k\| = 0$

$$
\begin{aligned}
\alpha_k &= r_k^T r_k / p_k^T A p_k \\
x_{k+1} &= x_k + \alpha_k p_k \\
r_{k+1} &= r_k + \alpha_k A p_k \\
\beta_{k+1} &= r_{k+1}^T r_{k+1} / r_k^T r_k \\
p_{k+1} &= -r_{k+1} + \beta_{k+1} p_k
\end{aligned}
$$

- Assignment：please implement CG method by C++ or Python, and test it on “iEDA/iPL”, submit by PR to iEDA repo.



Talent Training: Support Contest

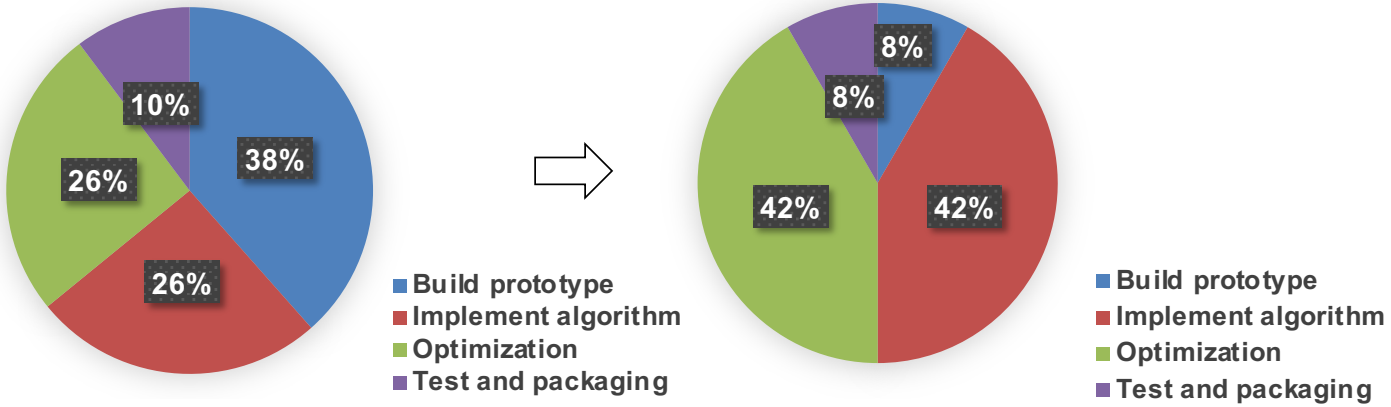
iEDA

文件 (4826)

- .gitee
- cmake
- contest
- docs
- scripts
- src
- .clang-format
- .clang-tidy
- .gitignore
- CMakeLists.txt
- LICENSE
- README-En.md
- README.md
- build.sh

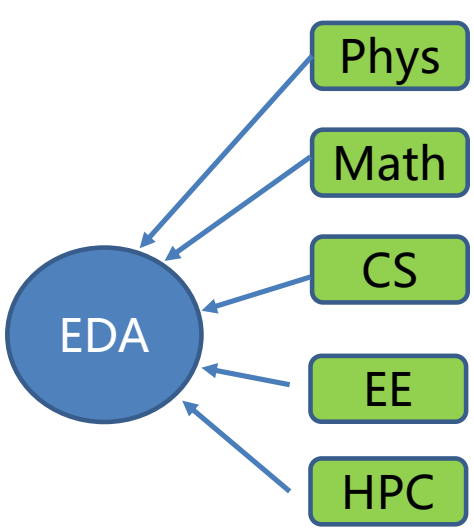
1st Place at 2022 ICCAD@ Contest

2st Place at 2023 ICCAD@ Contest

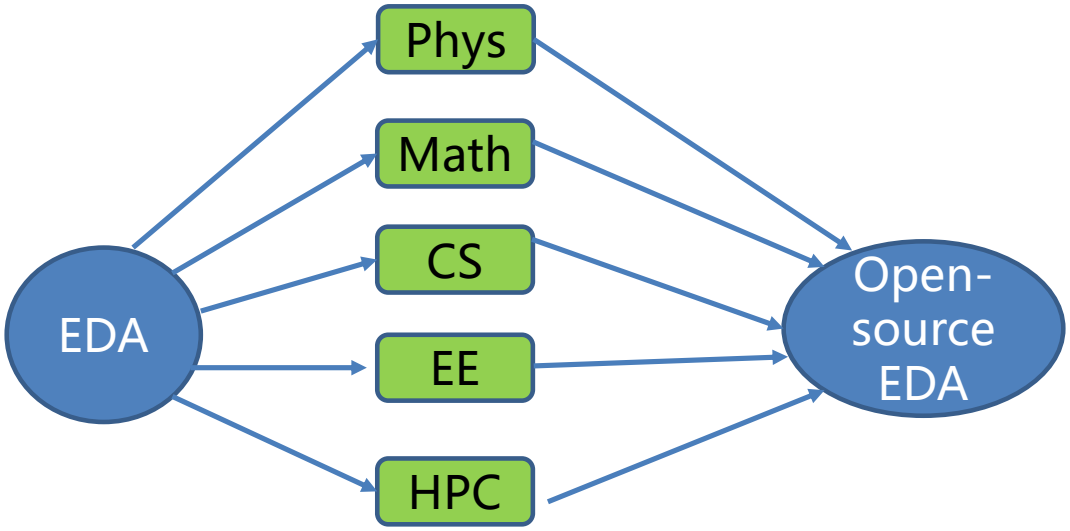


Proportion of time spent

Closed vs. Open

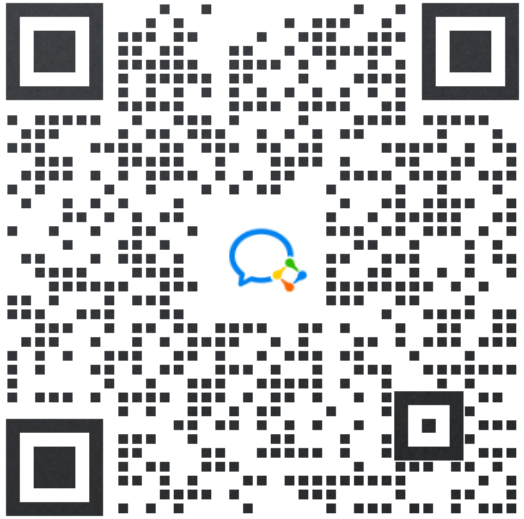


Closed-source EDA



Open-source EDA

WeChat Group:



Thanks

Welcome to join us

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