Semiconductors

The Final Frontier Of Open Source

by Daniel Bovensiepen

Open Source @ Siemens on 2023-05-24

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prolog

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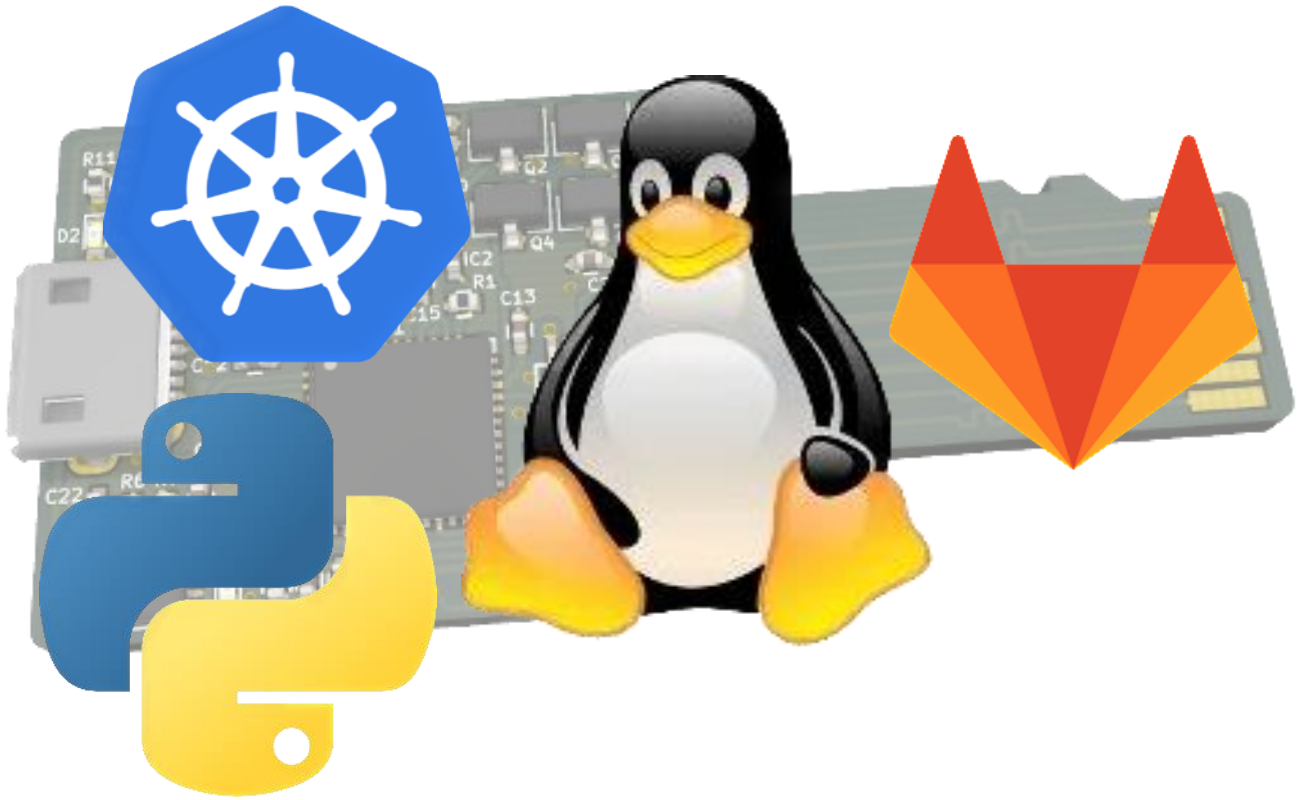
Open Source Software



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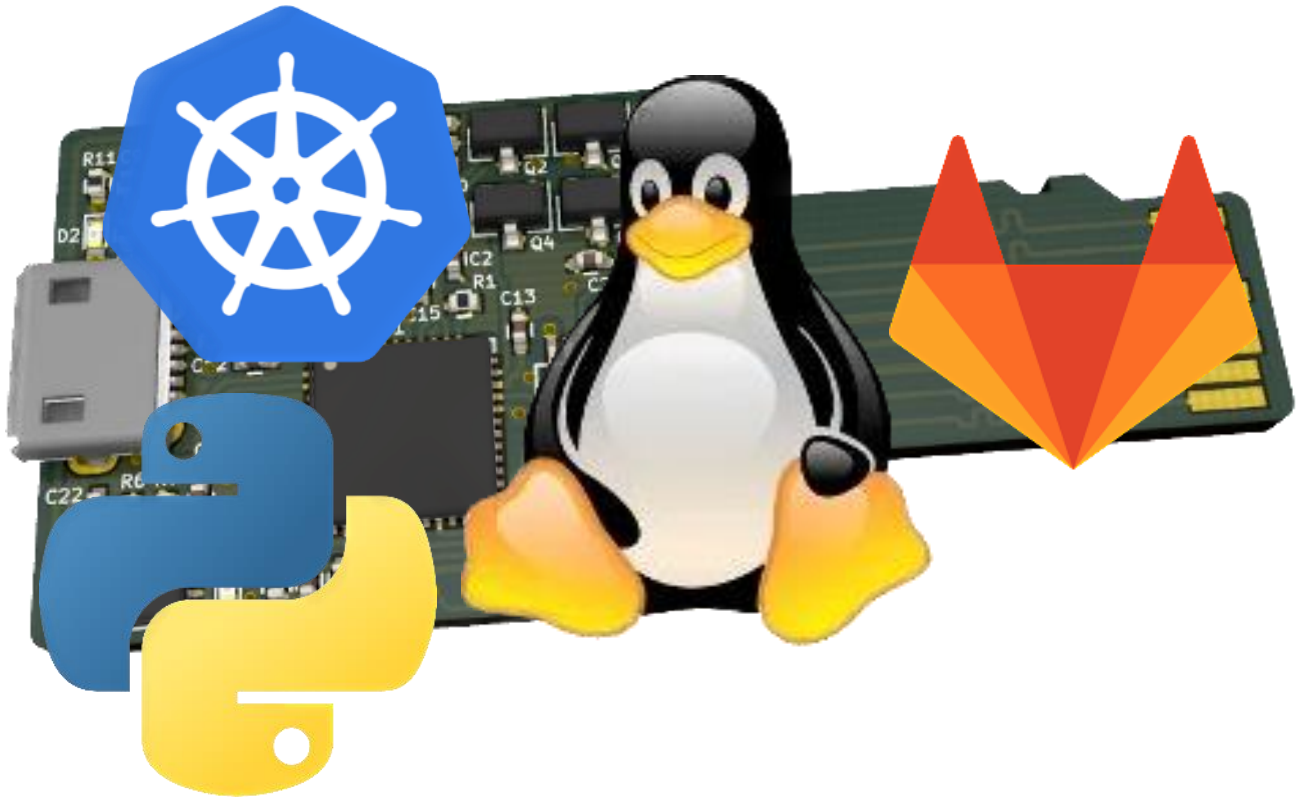
Open Source Hardware



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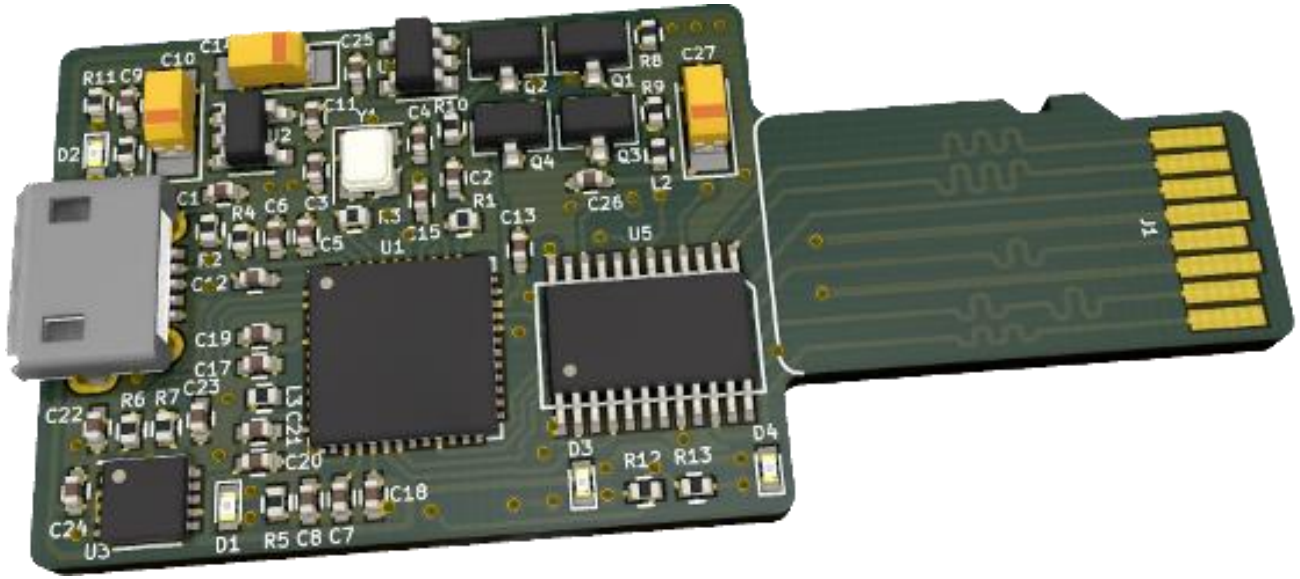
Open Source Semiconductors



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The Final Frontier Of Open Source

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Who am I and why do I talk about this?

Hi 👋
I'm Daniel Bovensiepen

👦💼 research on industrial communication

👦💻 open source stuff @ github.com/bovi

🗺 living in 北京

“thought-provoking” questions

1) Do you have basic knowledge how an ASIC is made?

2) Do you think an Open Source ASIC is possible today?

3) Do you dare to design your own ASIC?

ASIC design flow

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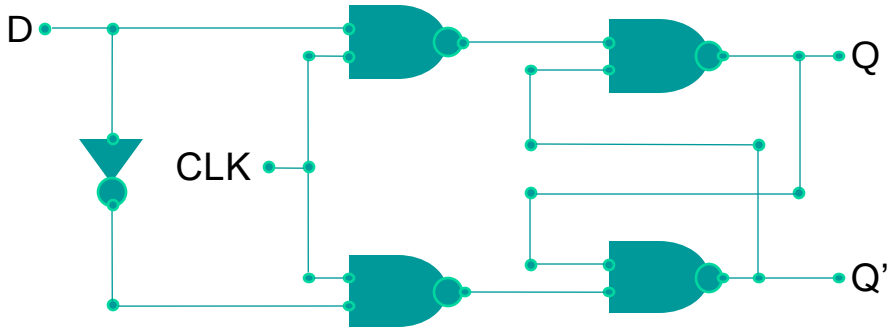
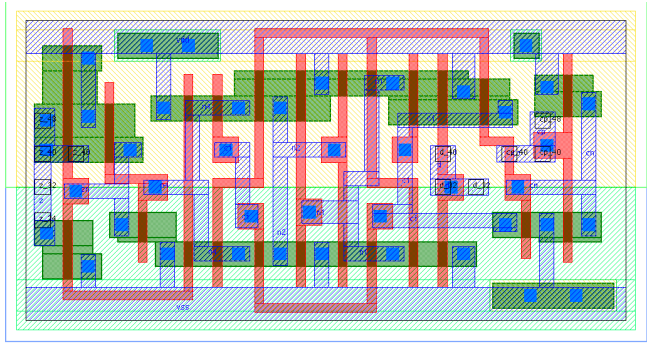
ASIC design flow

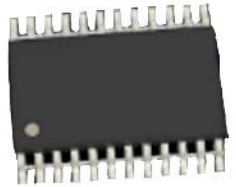
```
module nand_gate(c,a,b);
    input a,b;
    output c;
    assign c = ~(a&b);
endmodule

module not_gate(f,e);
    input e;
    output f;
    assign f= ~e;
endmodule

module d_ff_struct(q,qbar,d,clk);
    input d,clk;
    output q, qbar;
    not_gate not1(dbar,d);
    nand_gate nand1(x,clk,d);
    nand_gate nand2(y,clk,dbar);
    nand_gate nand3(q,qbar,y);
    nand_gate nand4(qbar,q,x);
endmodule
```







ASIC

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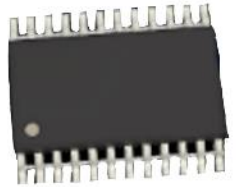
ASIC design flow

```
module nand_gate(c,a,b);
    input a,b;
    output c;
    assign c = ~(a&b);
endmodule

module not_gate(f,e);
    input e;
    output f;
    assign f= ~e;
endmodule

module d_ff_struct(q,qbar,d,clk);
    input d,clk;
    output q, qbar;
    not_gate not1(dbar,d);
    nand_gate nand1(x,clk,d);
    nand_gate nand2(y,clk,dbar);
    nand_gate nand3(q,qbar,y);
    nand_gate nand4(qbar,q,x);
endmodule
```



ASIC

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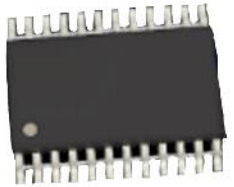
ASIC design flow

Design

Fab

Tapeout



ASIC

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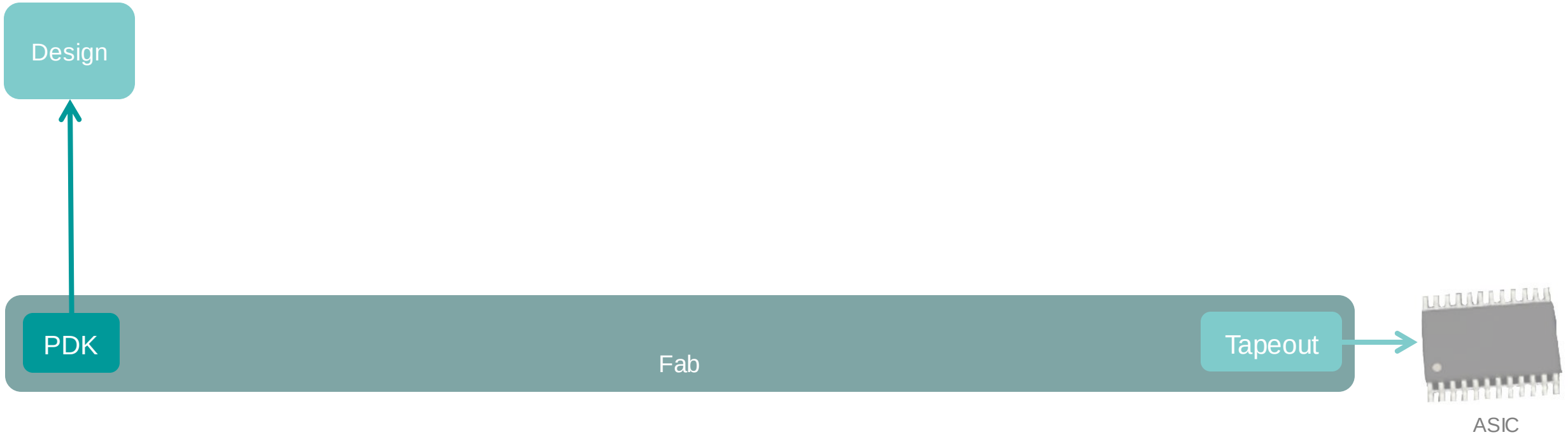
ASIC design flow



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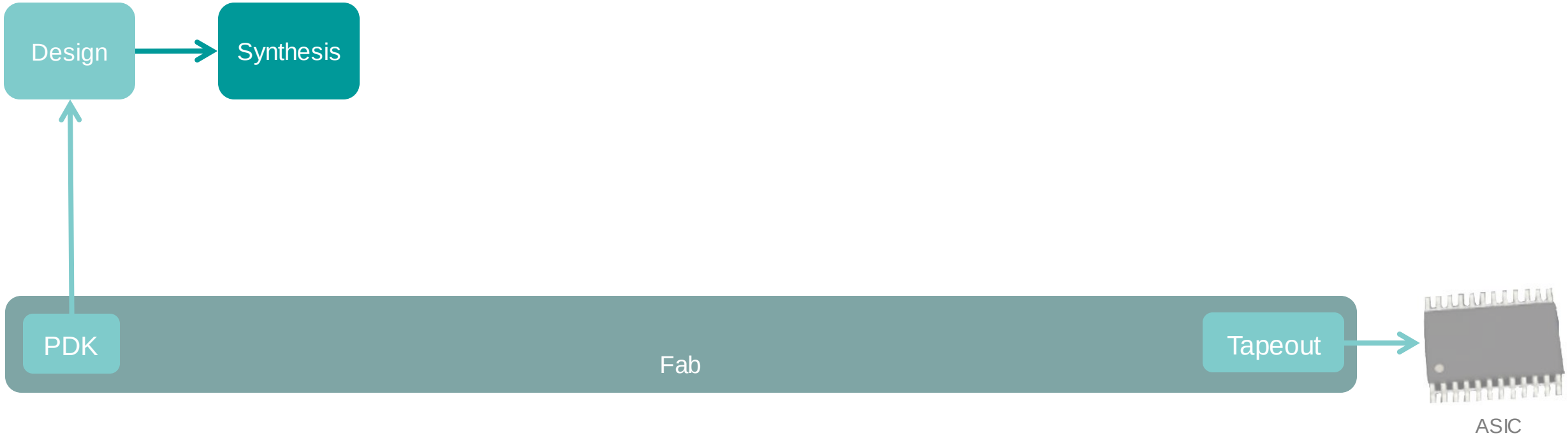
ASIC design flow



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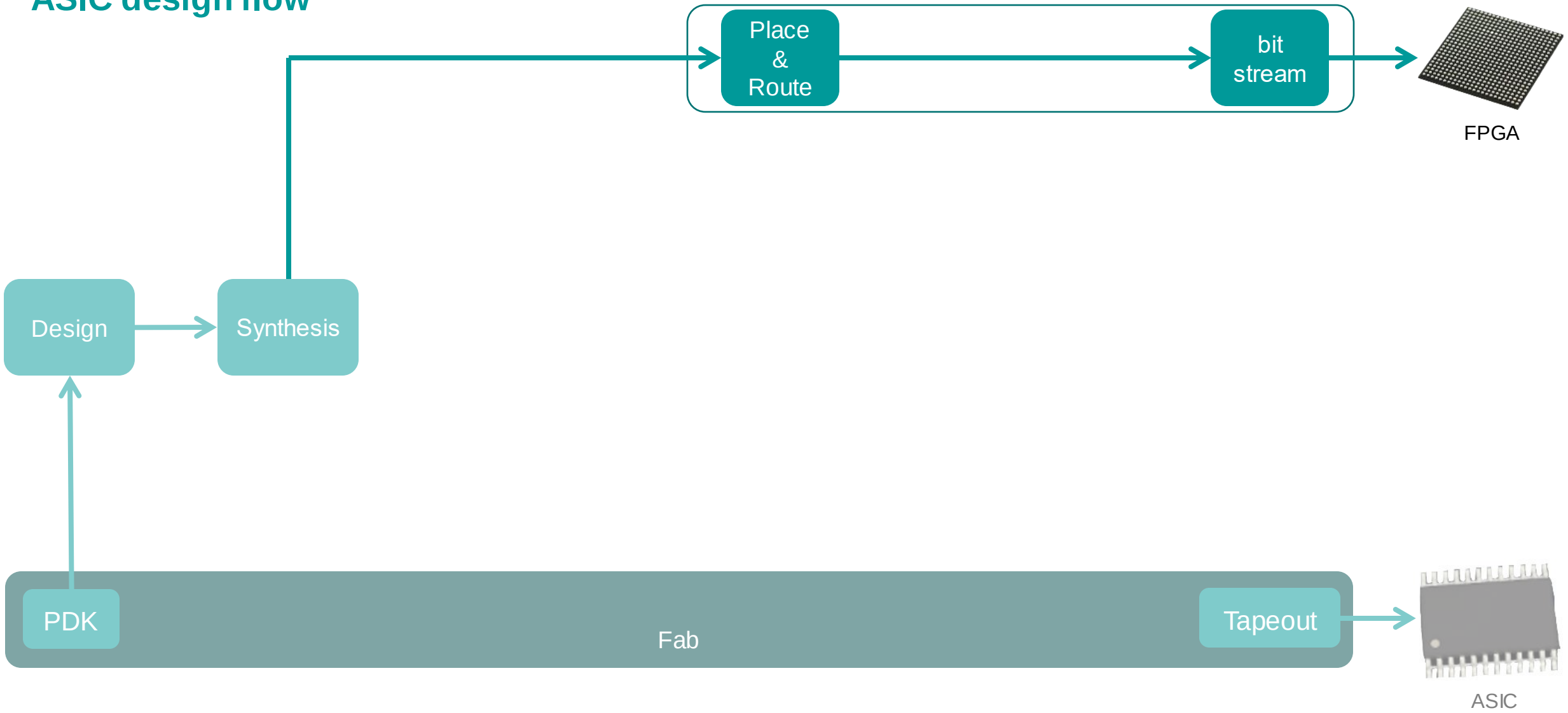
ASIC design flow



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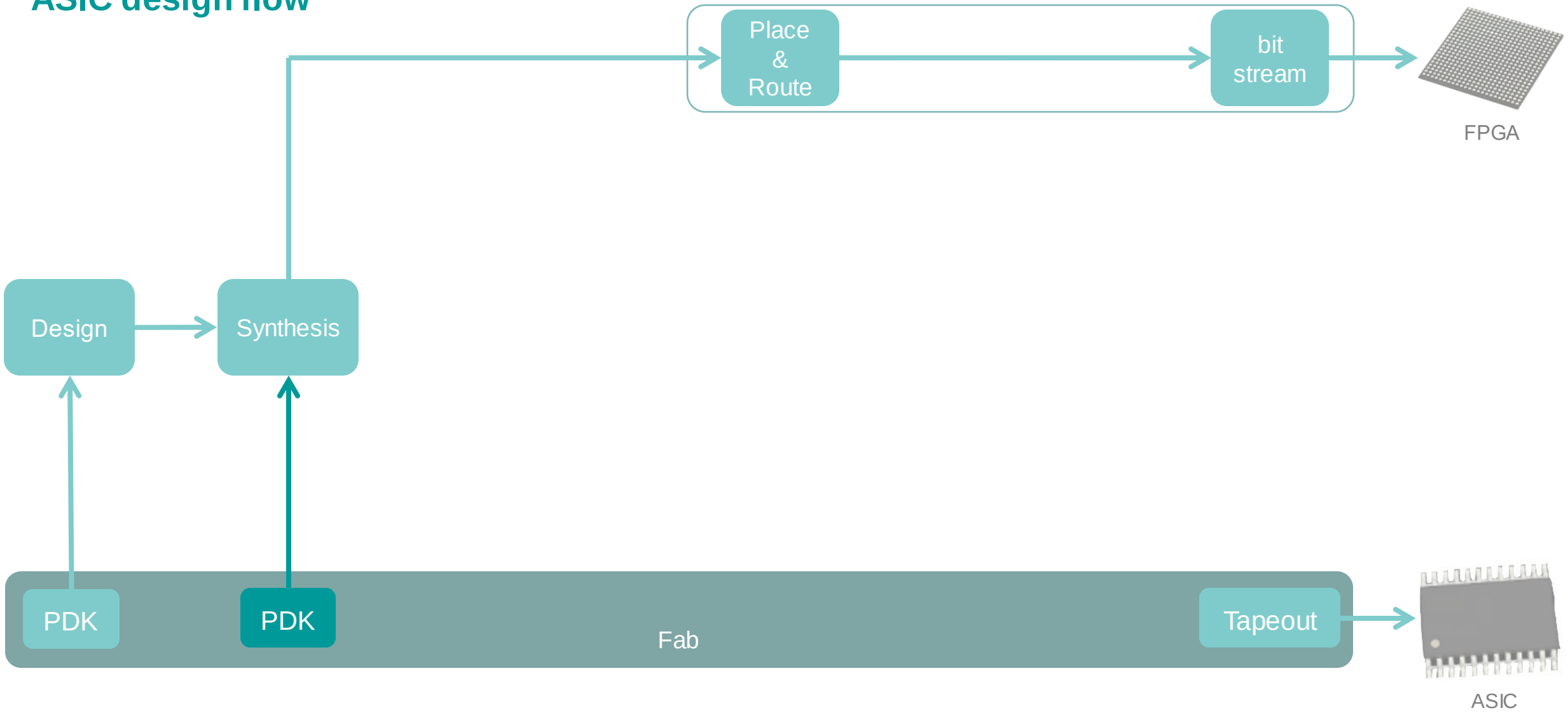
ASIC design flow



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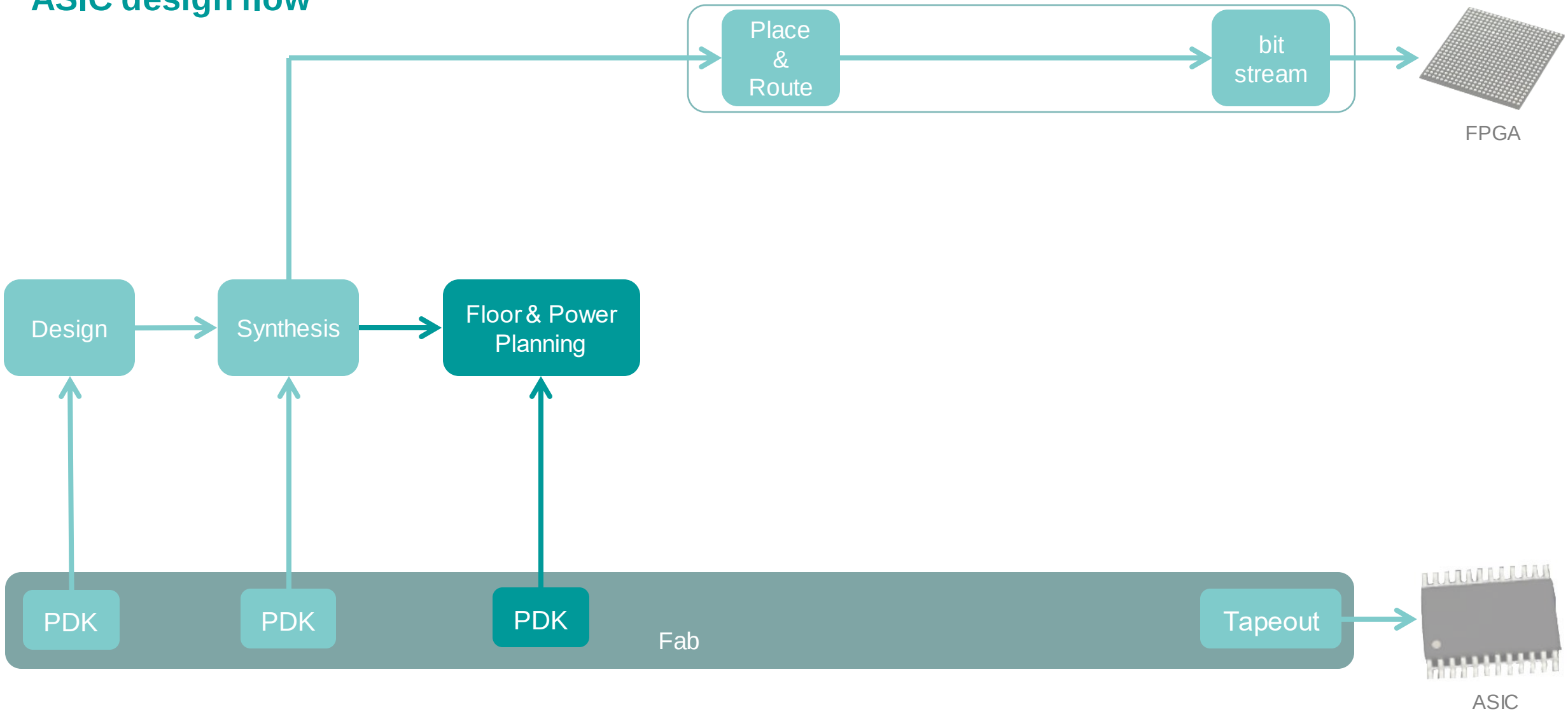
ASIC design flow



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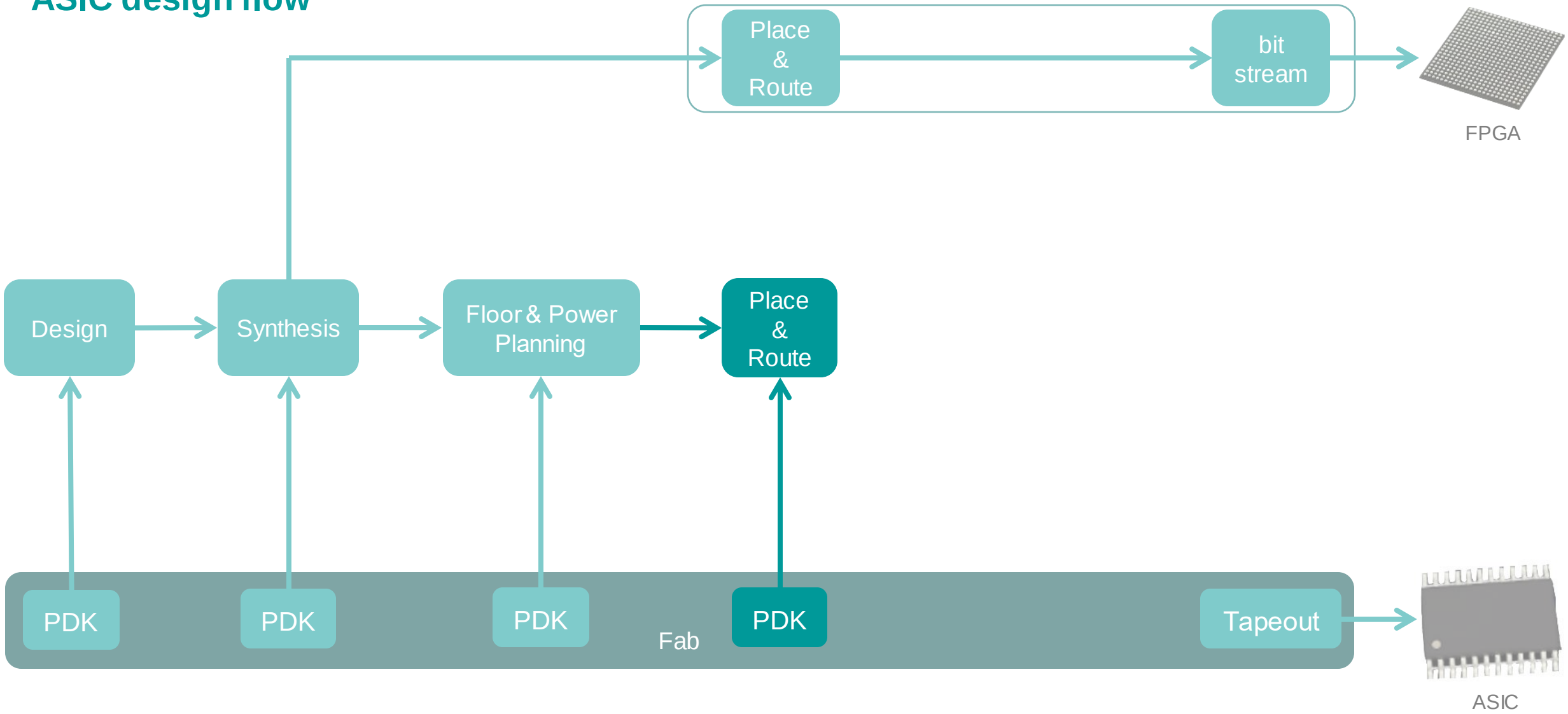
ASIC design flow



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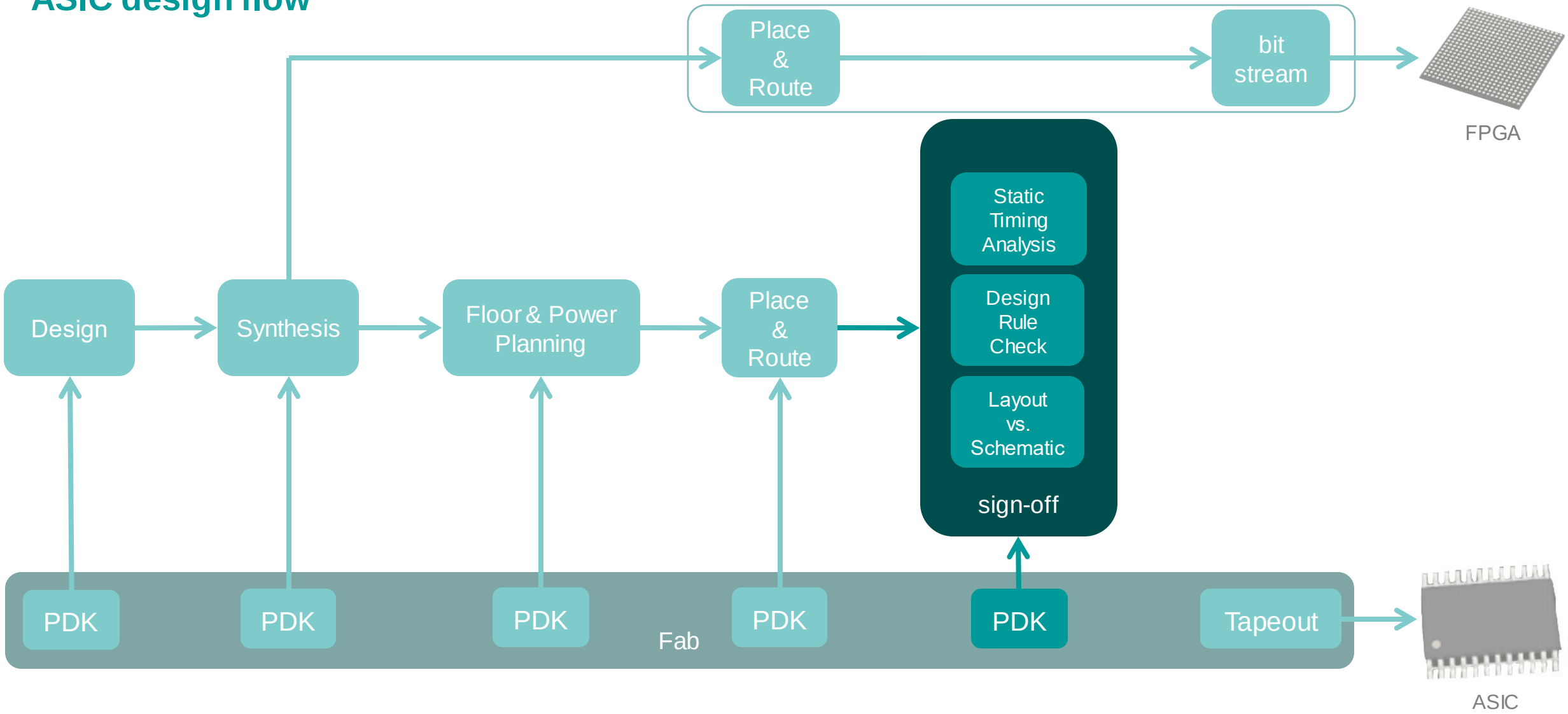
ASIC design flow



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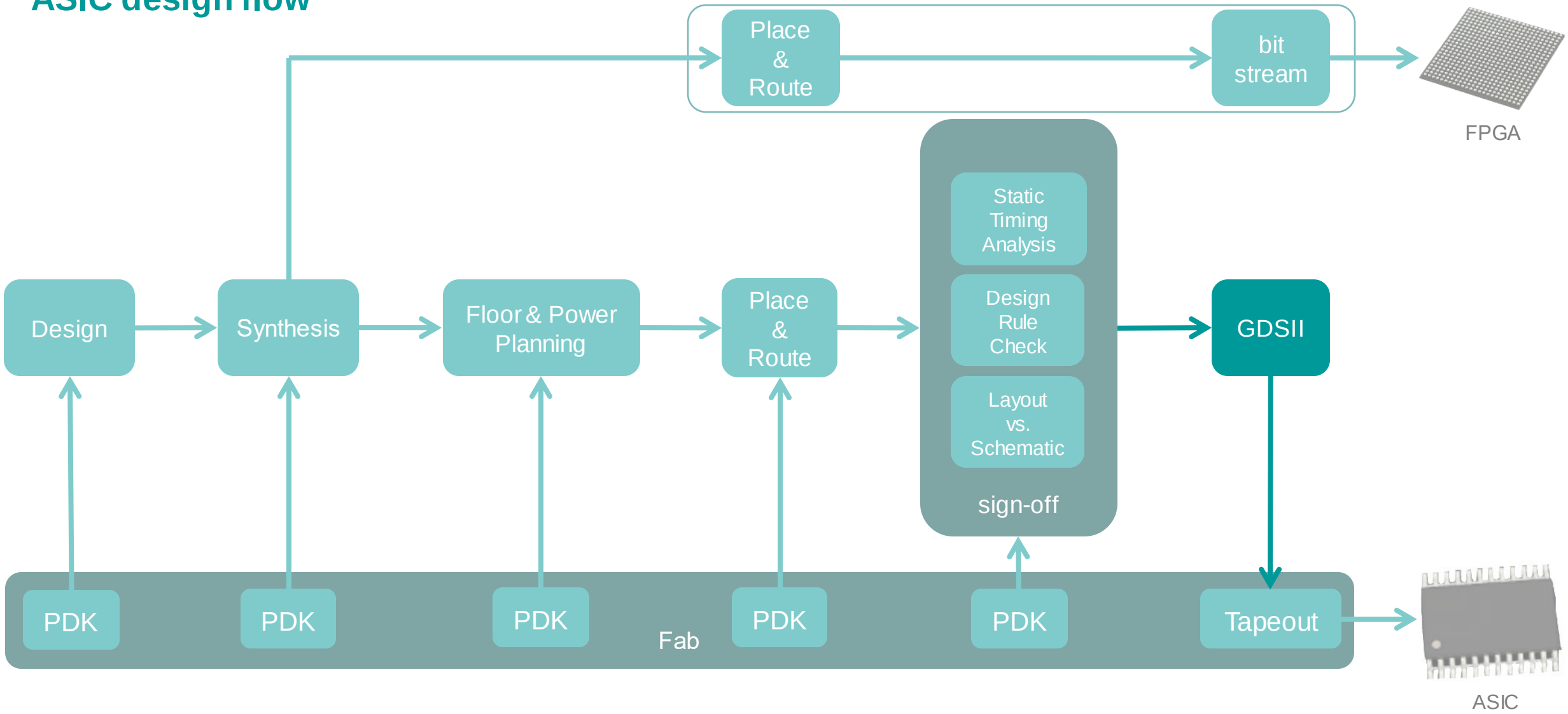
ASIC design flow



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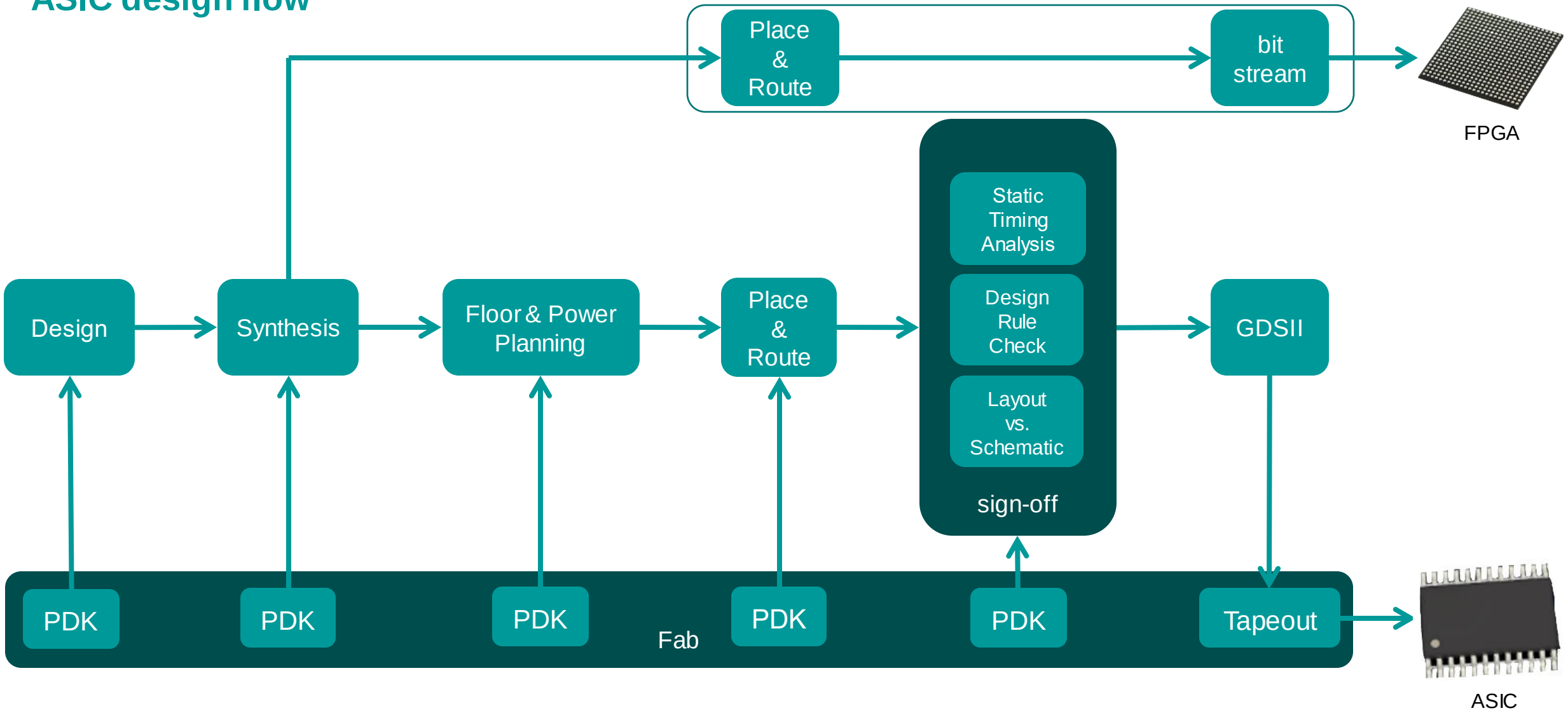
ASIC design flow



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Open Source ASIC design flow

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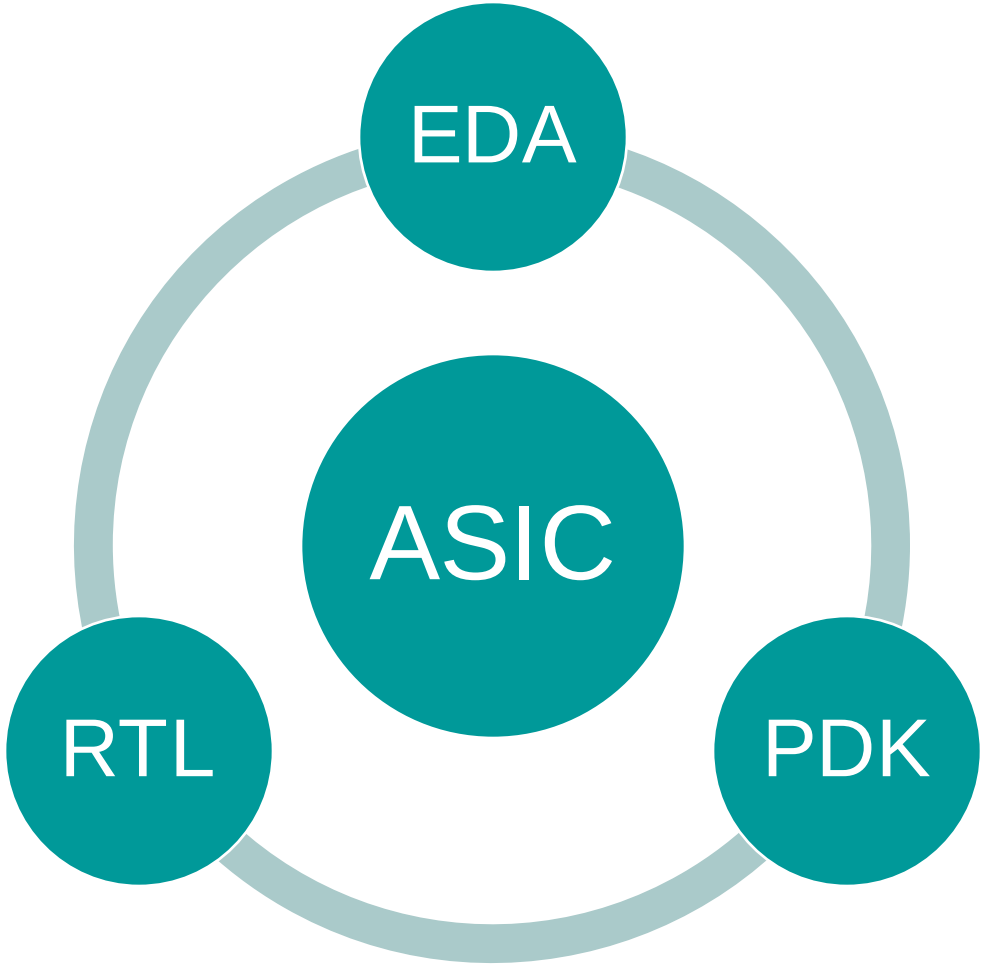
The three pillars of ASIC design



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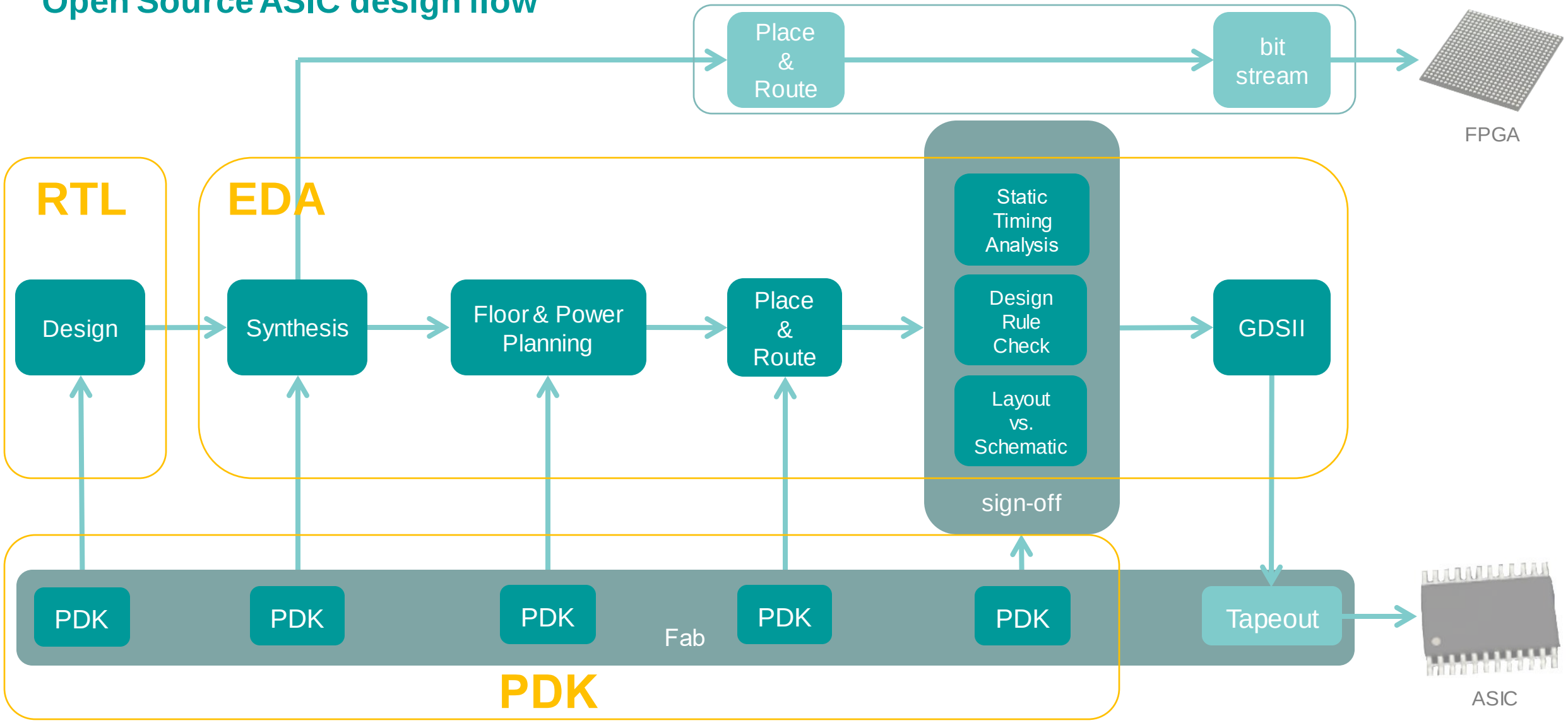
Open Source ASIC design flow



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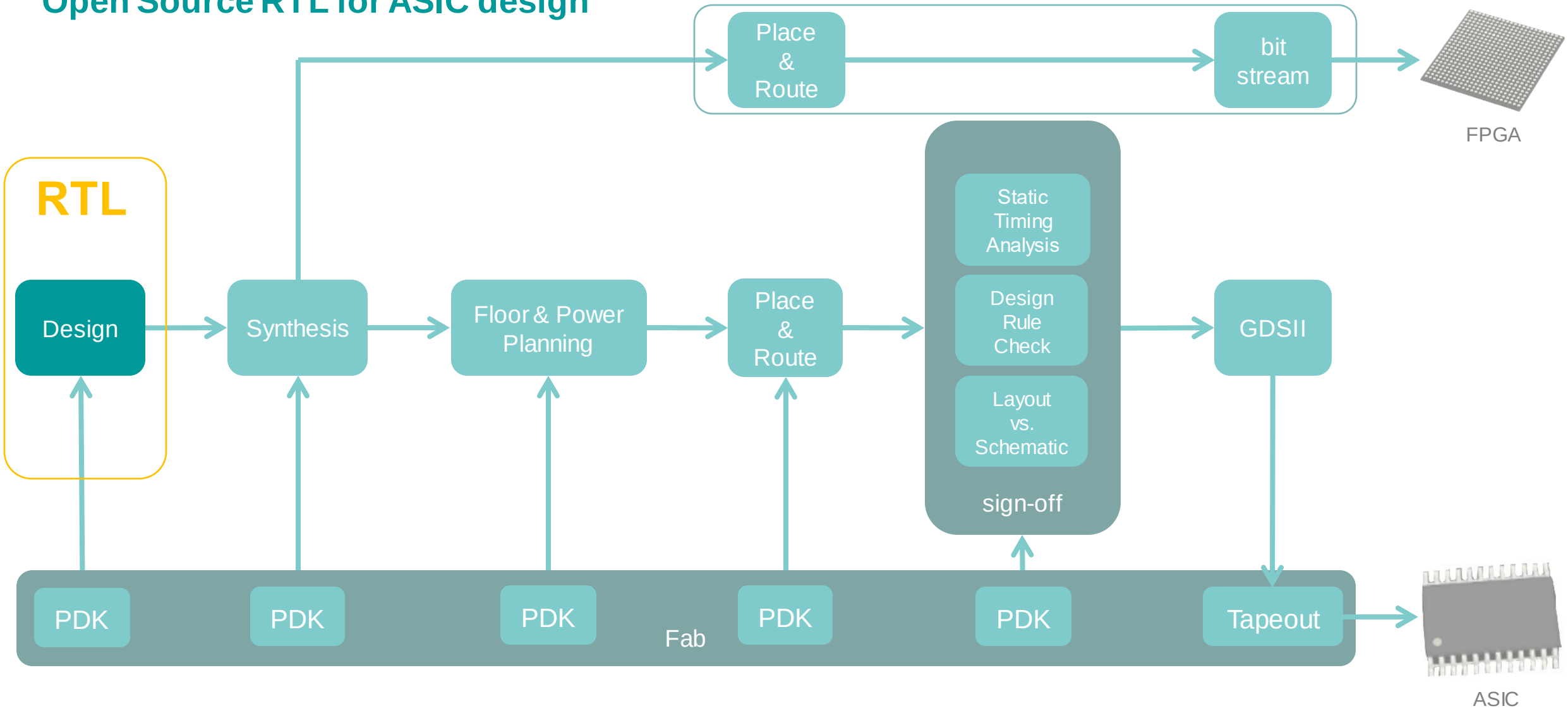
Open Source RTL for ASIC design



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Open Source RTL for ASIC design

Hardware Description Languages (HDL)

Verilog

Bluespec

Amaranth HDL

VHDL

SpinalHDL

CHISEL

Intellectual Property Cores (IP Cores)

picorv32

OpenRAM

FASoC

Design Communities

opencores.org

~~librecores.org~~

github.com

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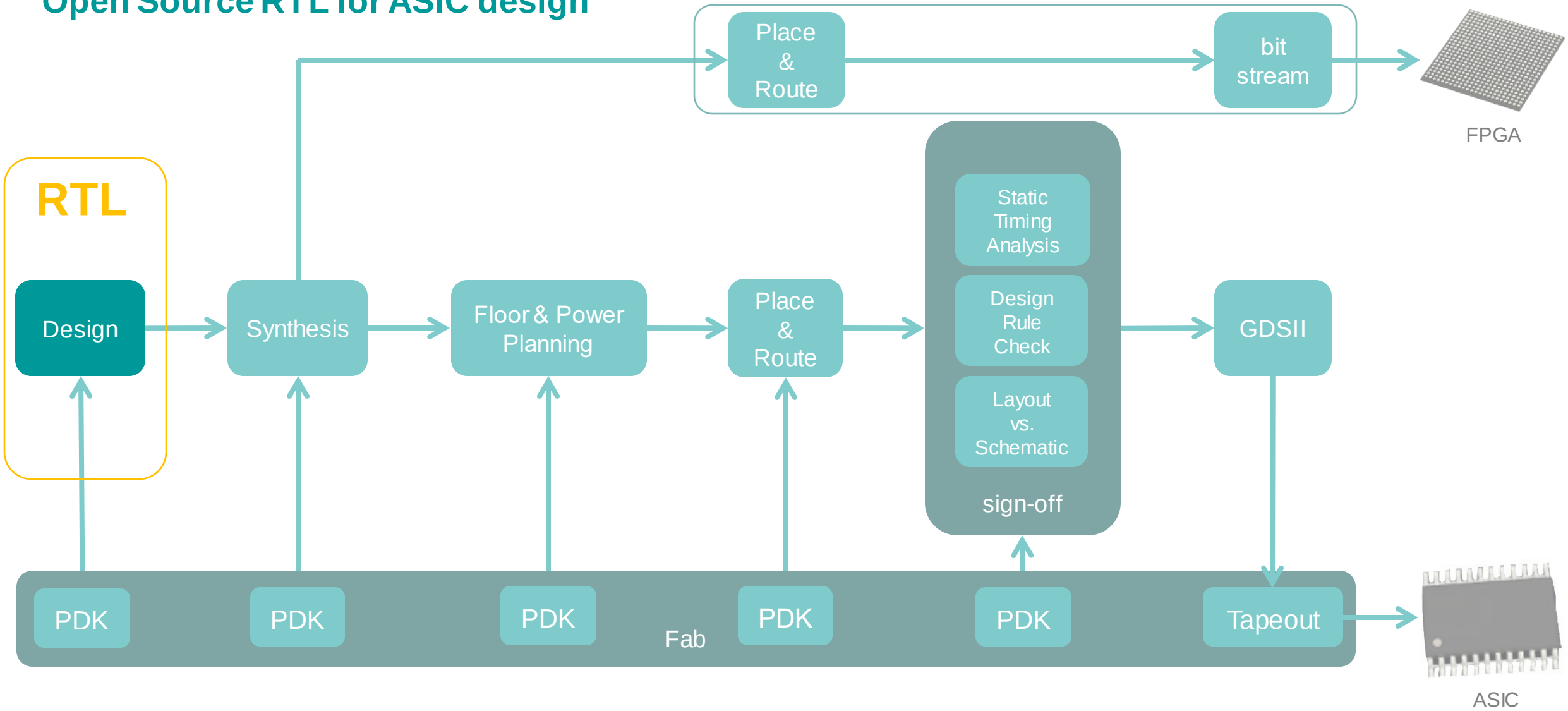
Open Source RTL for ASIC design



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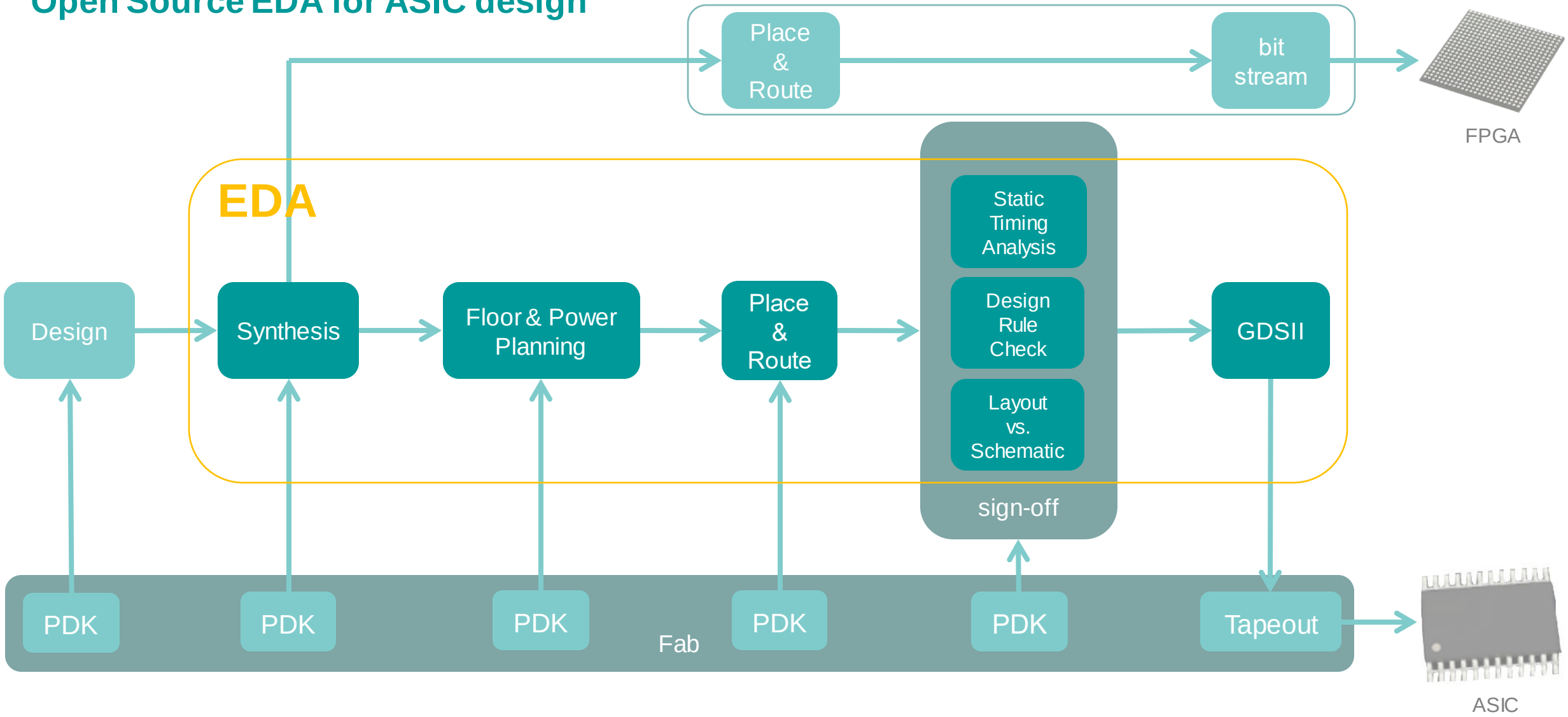
Open Source EDA for ASIC design



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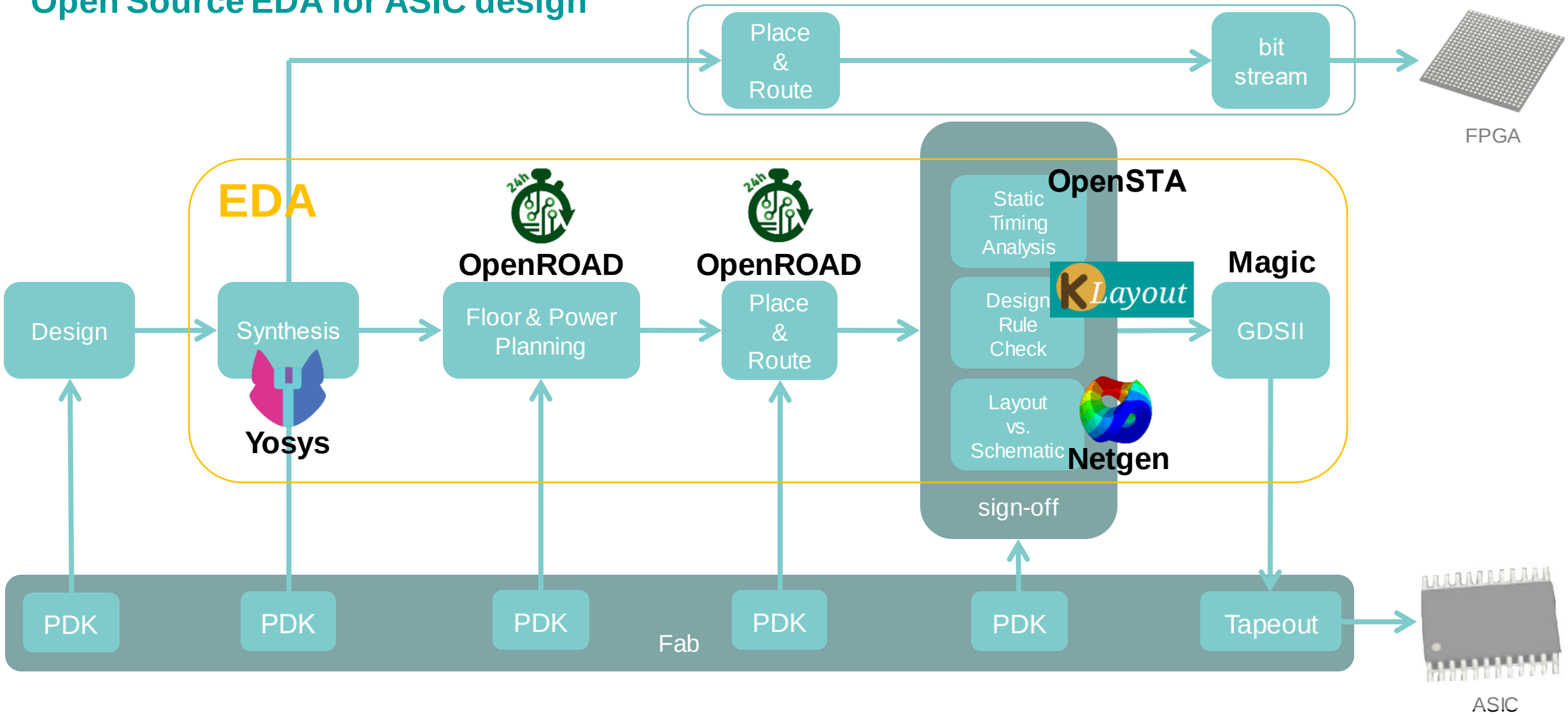
Open Source EDA for ASIC design



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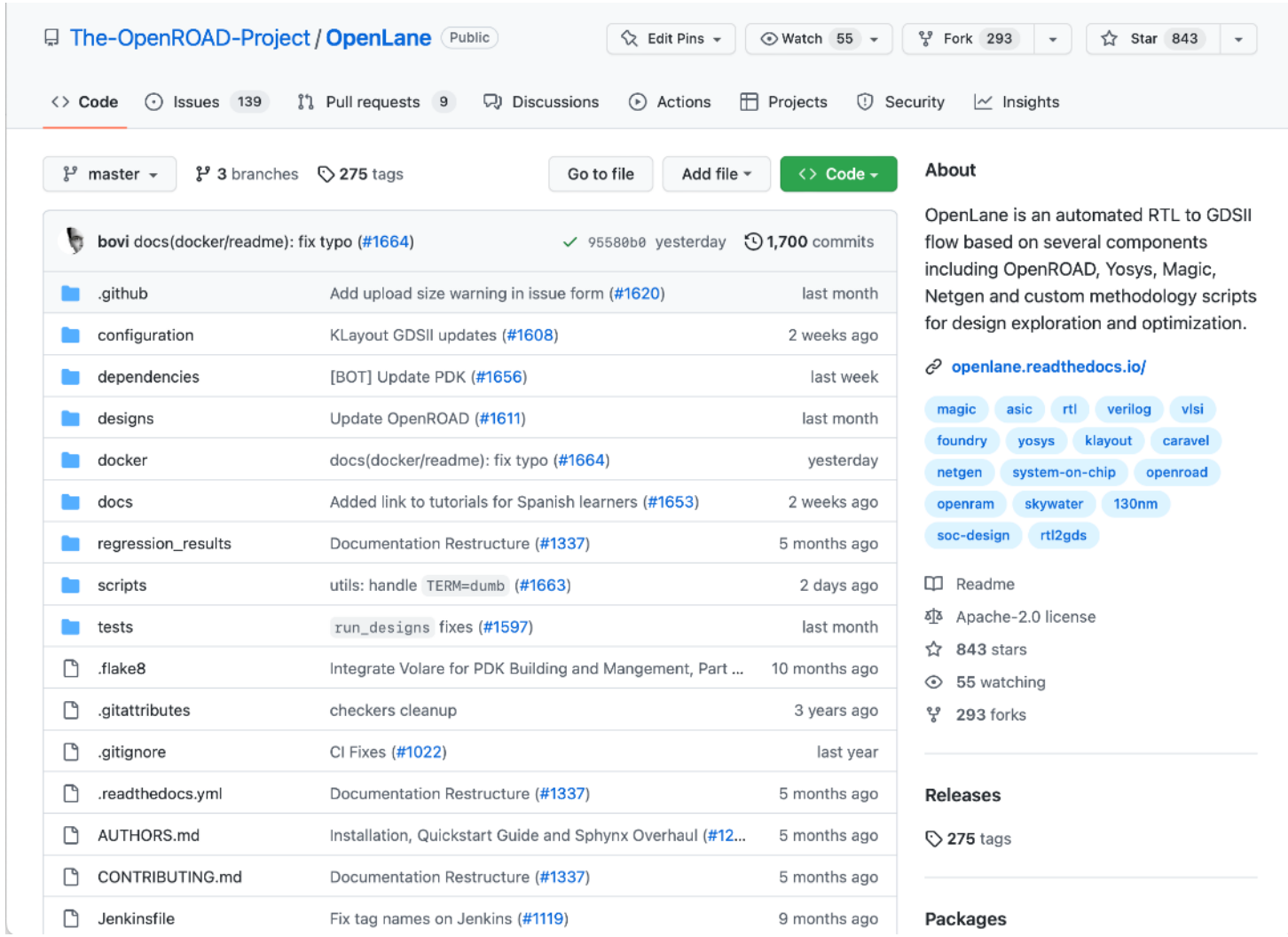
Open Source EDA for ASIC design

OpenLane is an automated RTL to GDSII flow based on several components including **OpenROAD**, **Yosys**, **Magic**, **Netgen** and custom methodology scripts for design exploration and optimization.



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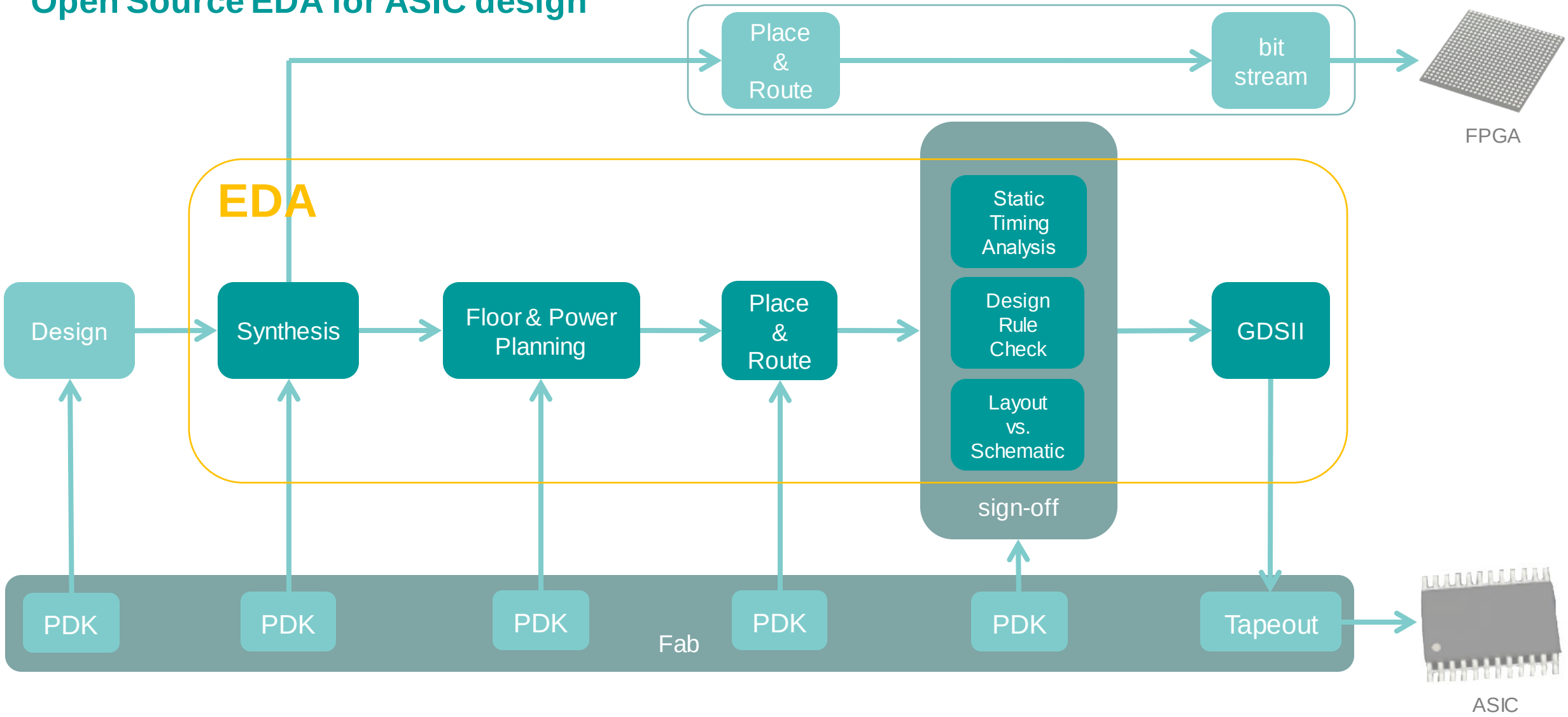
Open Source EDA for ASIC design



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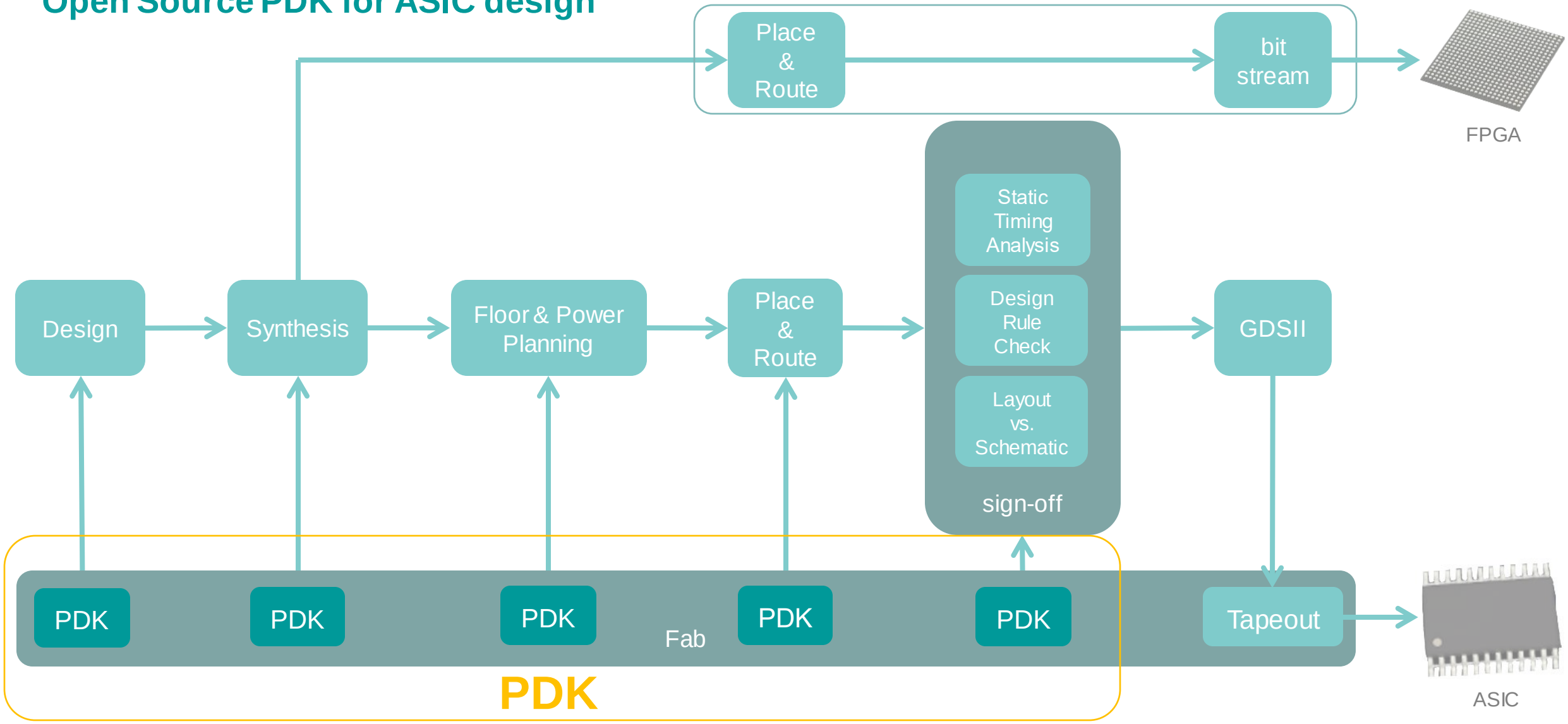
Open Source PDK for ASIC design



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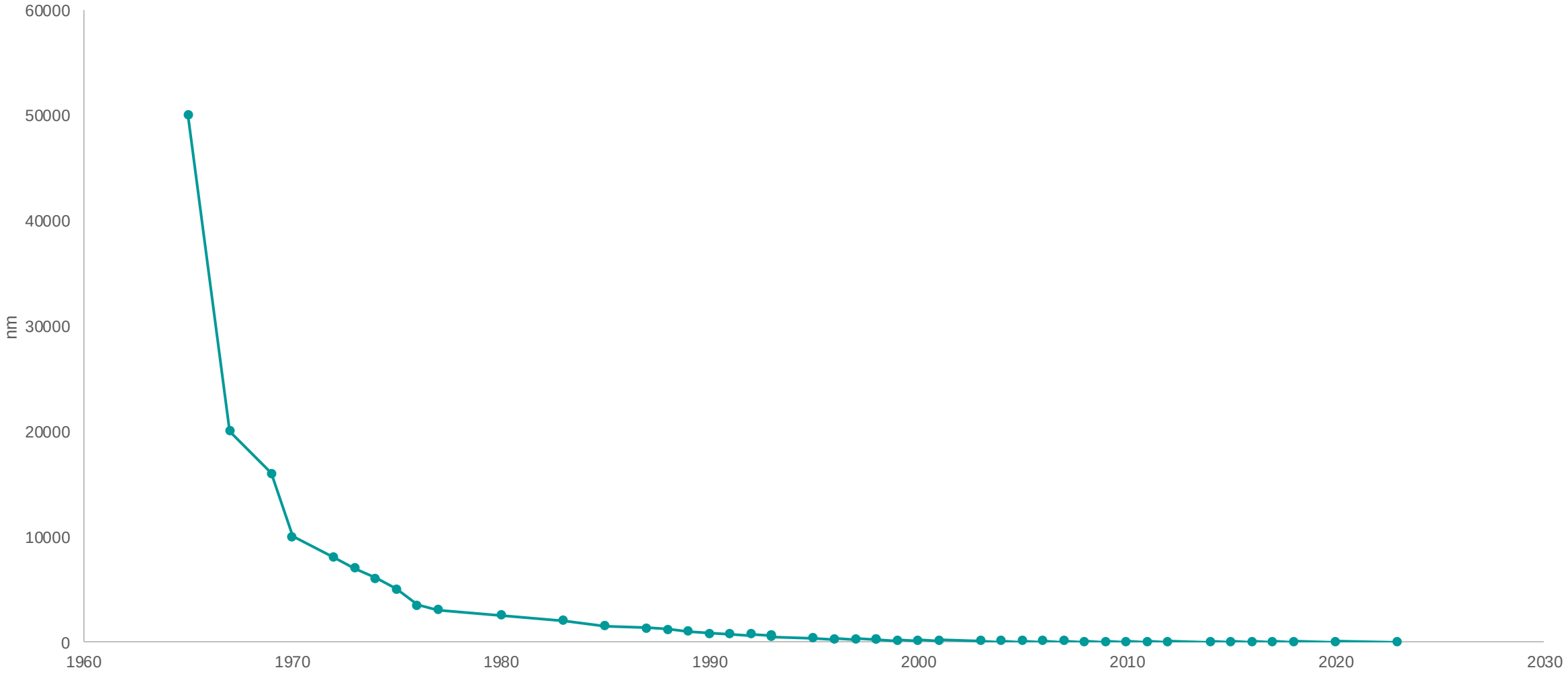
Process nodes from ~1960 to ~2020



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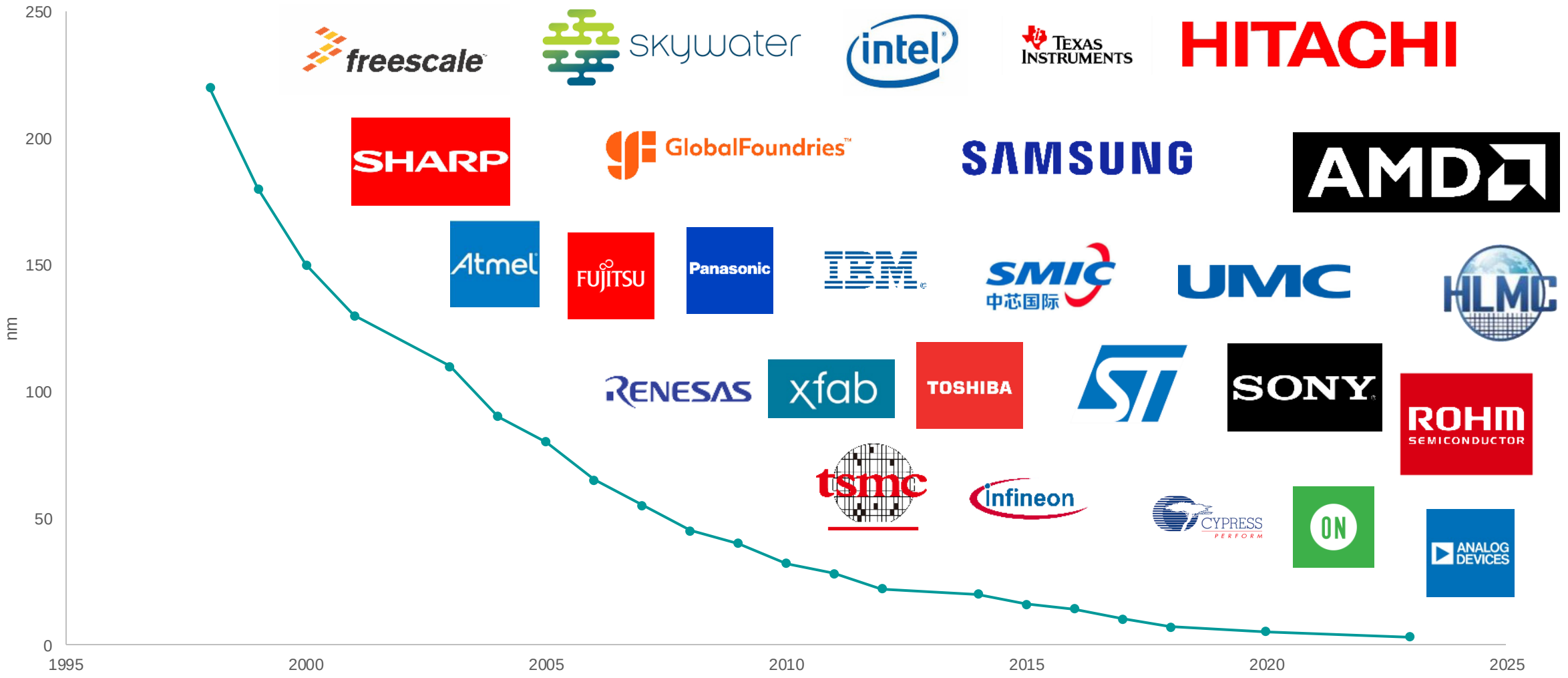
Process nodes from ~2000 to ~2020



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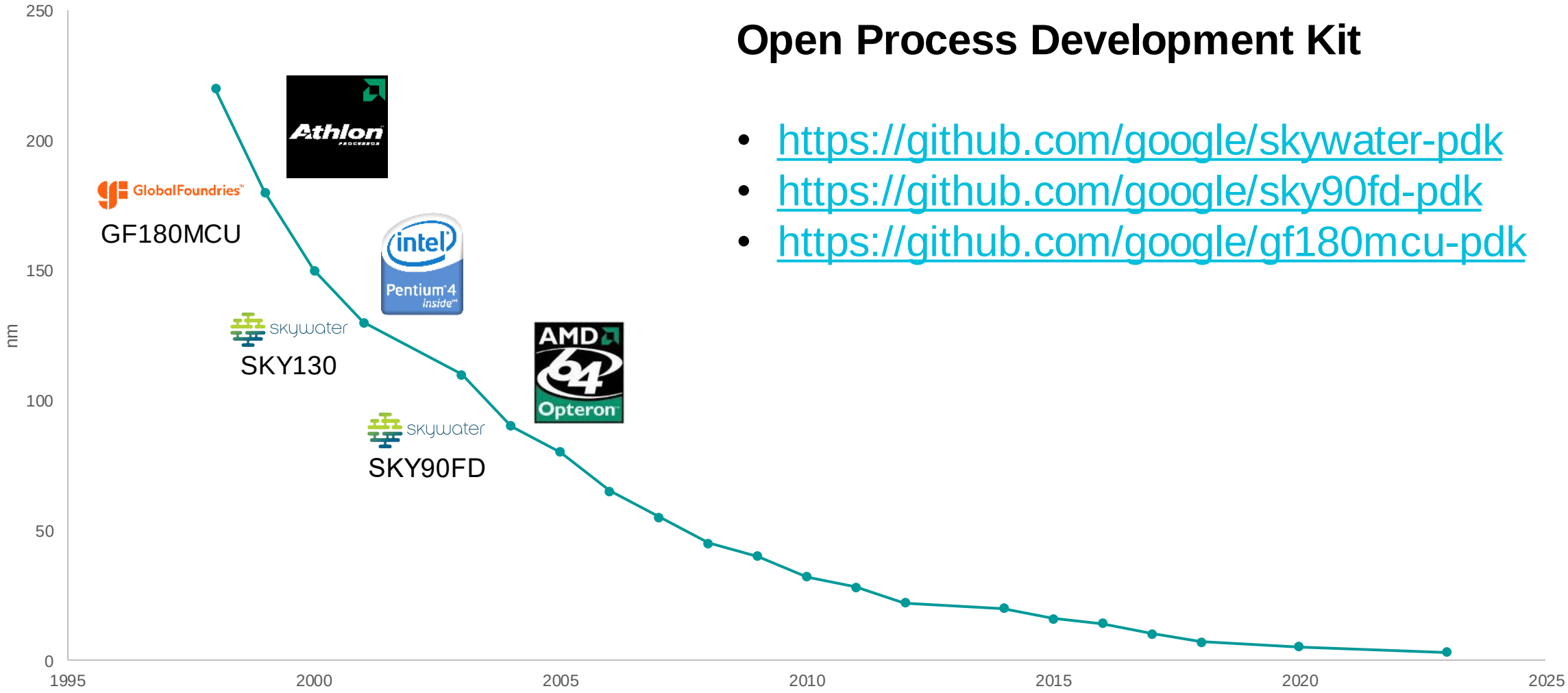
Process nodes from ~2000 to ~2020



Open Process Development Kit

- https://github.com/google/skywater-pdk
- https://github.com/google/sky90fd-pdk
- https://github.com/google/gf180mcu-pdk

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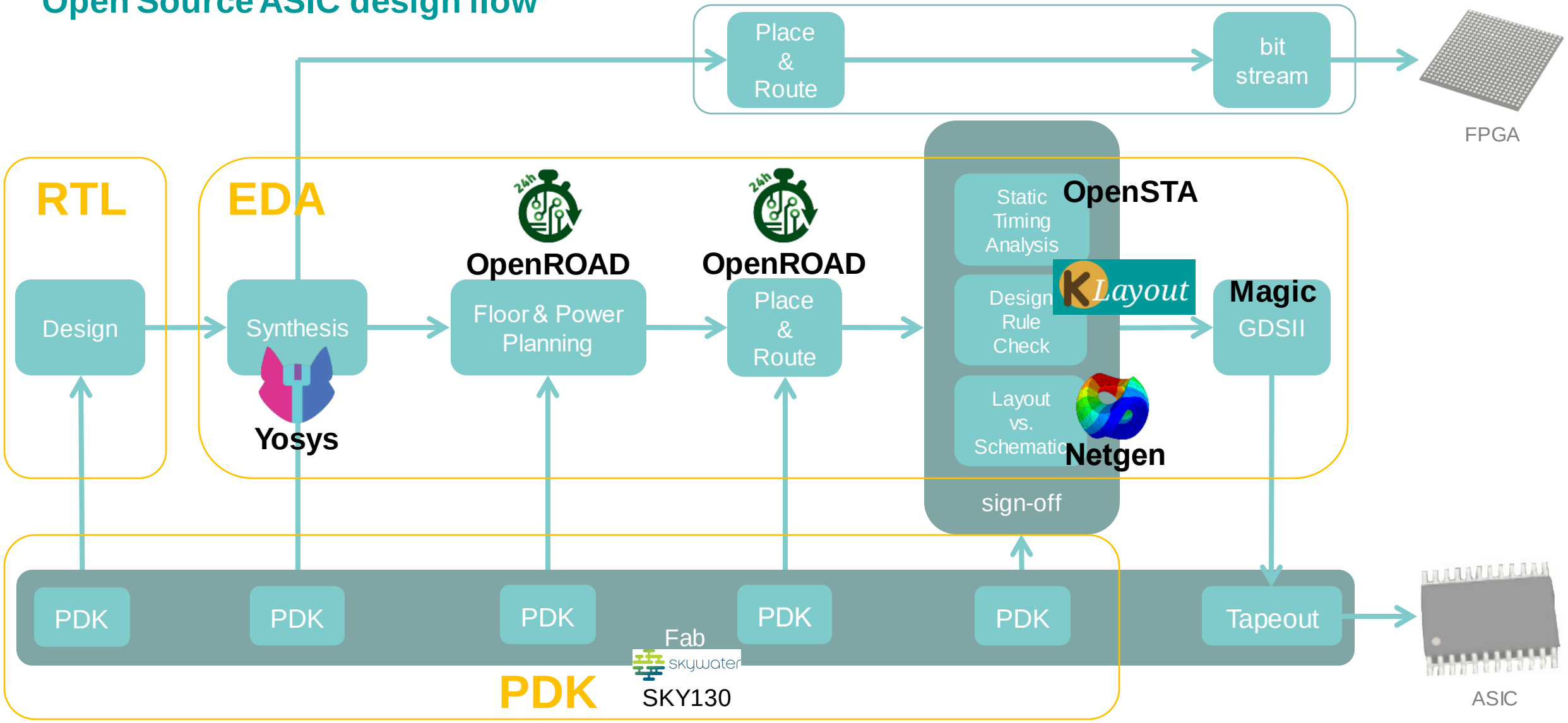
Open Source ASIC design flow



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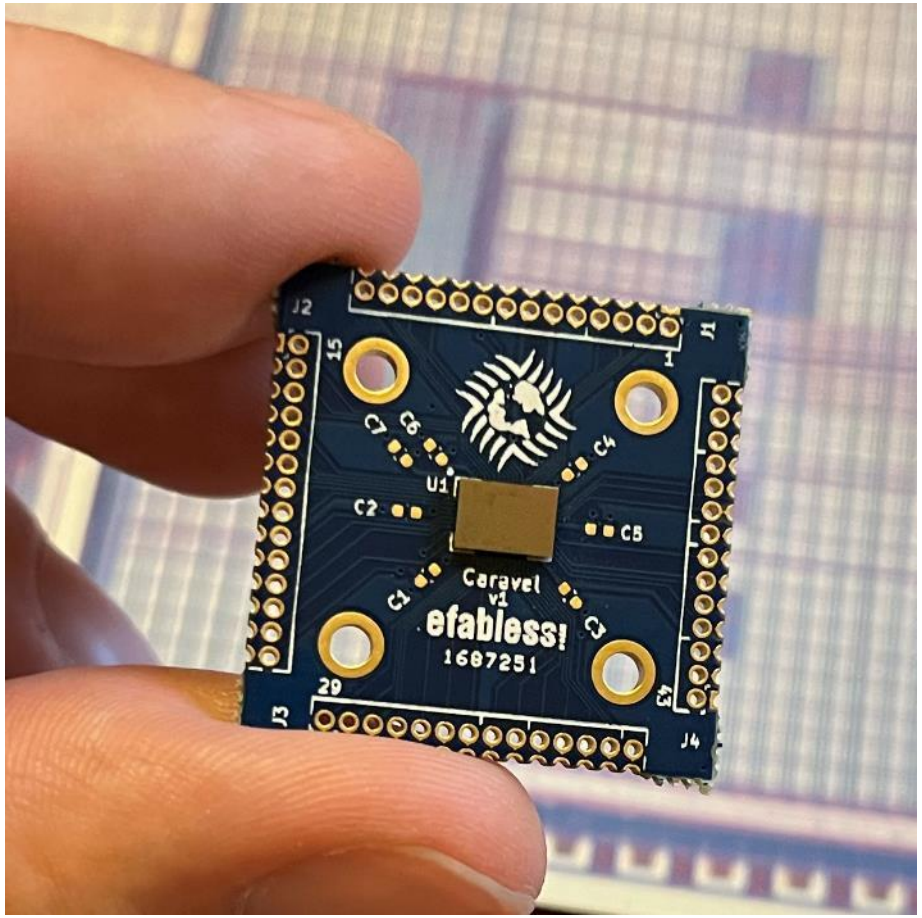
Can we build an Open Source ASIC?



yes we can

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How to build your own ASIC

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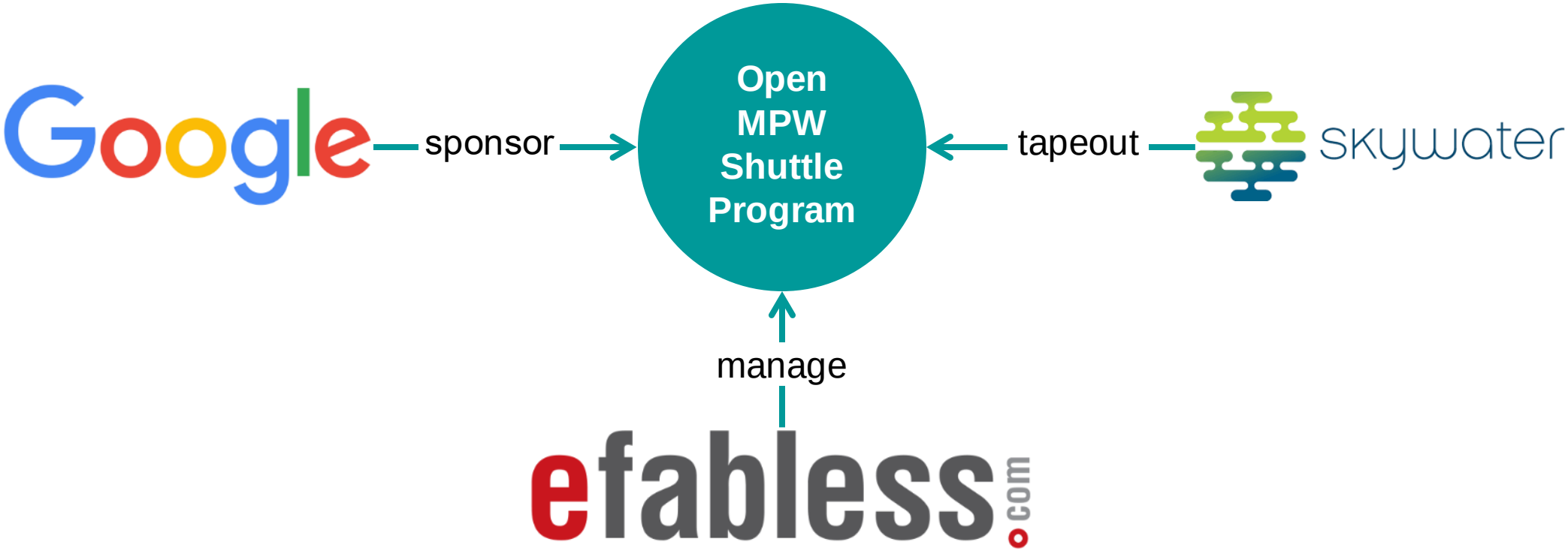
Open Multi Project Wafer Shuttle Program

Program details

- 8 shuttles
- 40 designs per shuttle
- 10mm² for each design
- everything is/must be Open Source



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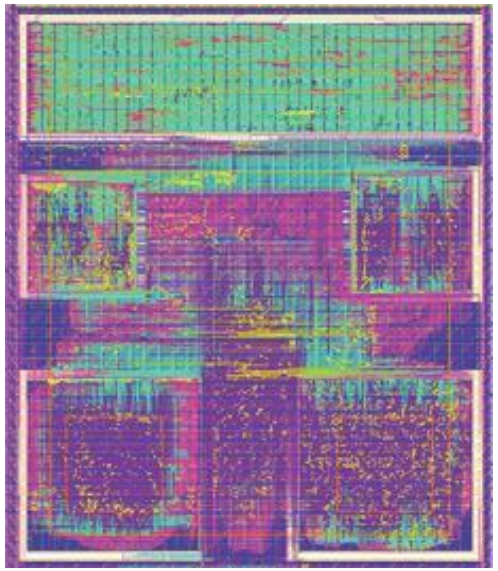
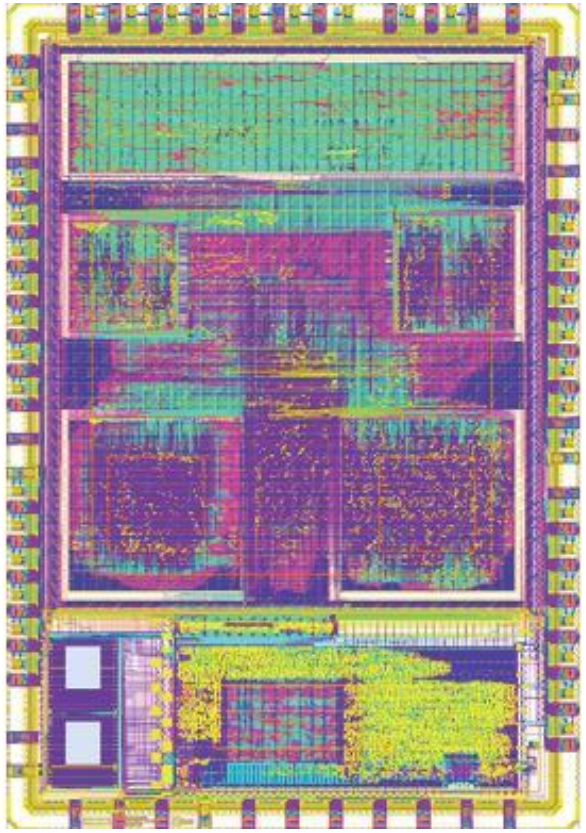
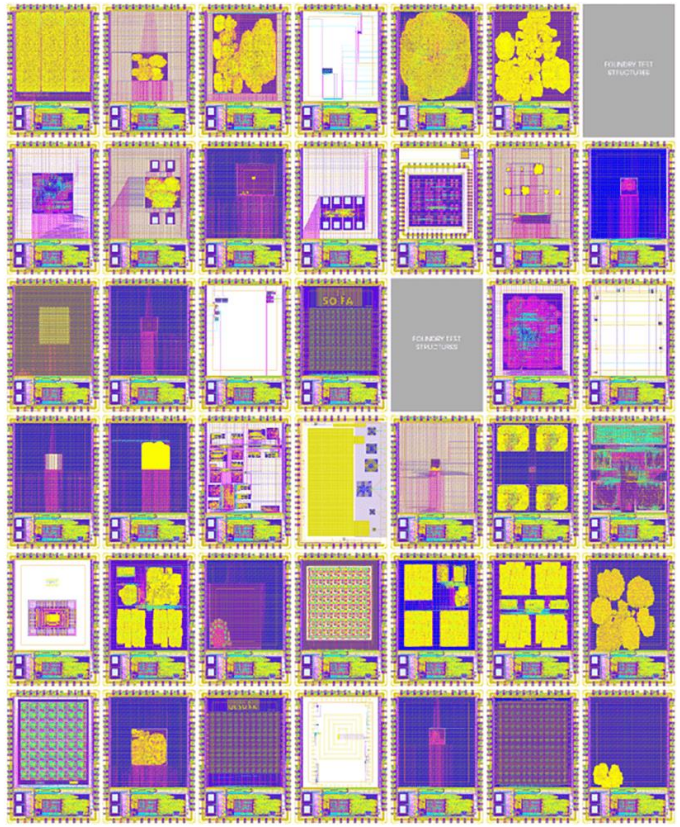
Open Multi Project Wafer Shuttle Program







Project Design

Caravel Harness with Project Design

Multi Project Integration

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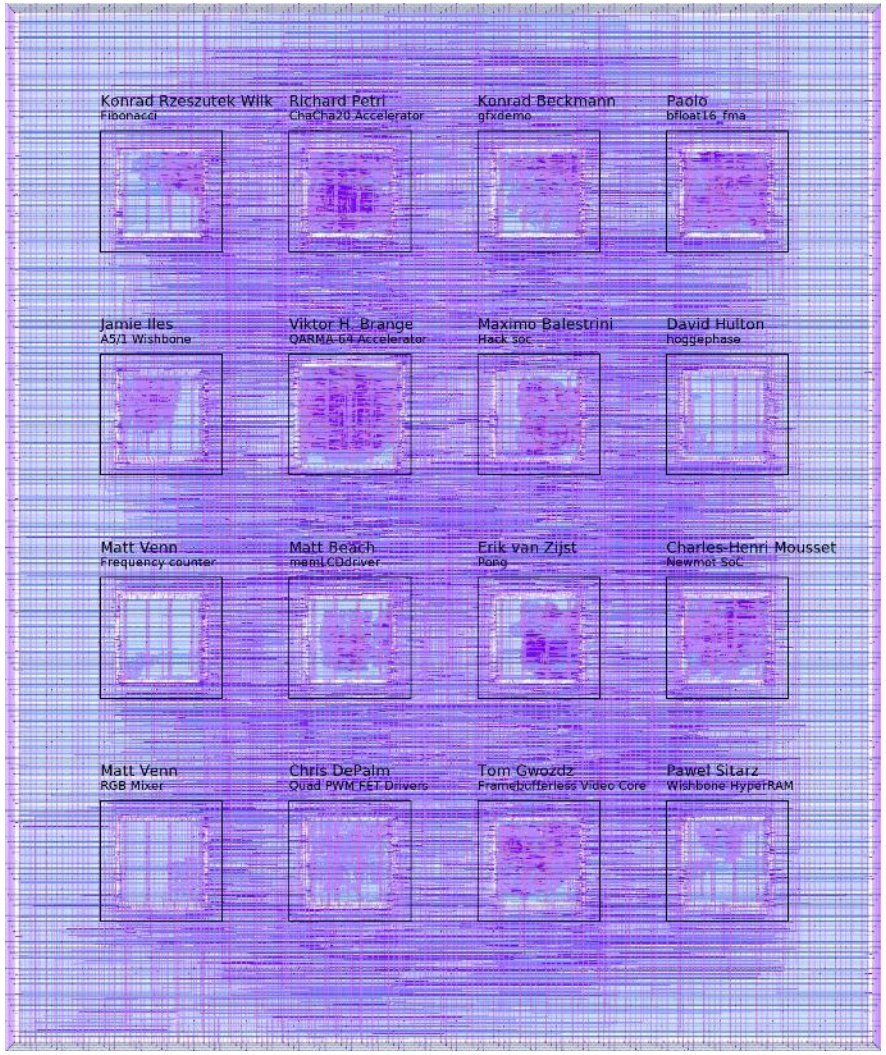
Zero 2 ASIC

Program details

- based on the Open MPW shuttle program
- 16 designs per Caravel user-space
- 300µm² for each design
- multi-project Caravel: https://github.com/mattvenn/caravel-mph

Organized by @matthewvenn



16 projects in one Caravel user space for MPW-2

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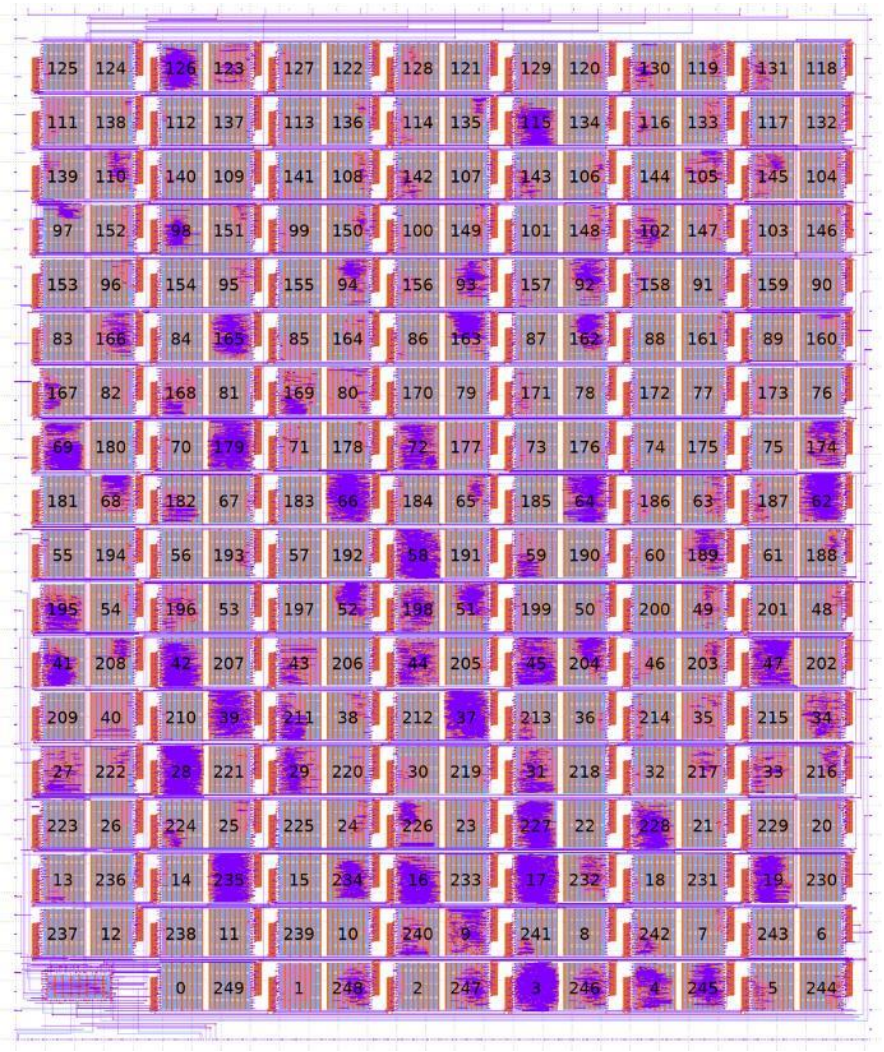
Tiny Tapeout

Program details

- tapeout guarantee with payment (25$ for design / 100$ for IC&PCB)
- 249 designs per Caravel user-space
- 150µm * 170µm for each design

Organized by
@matthewvenn



249 projects in one Caravel user space

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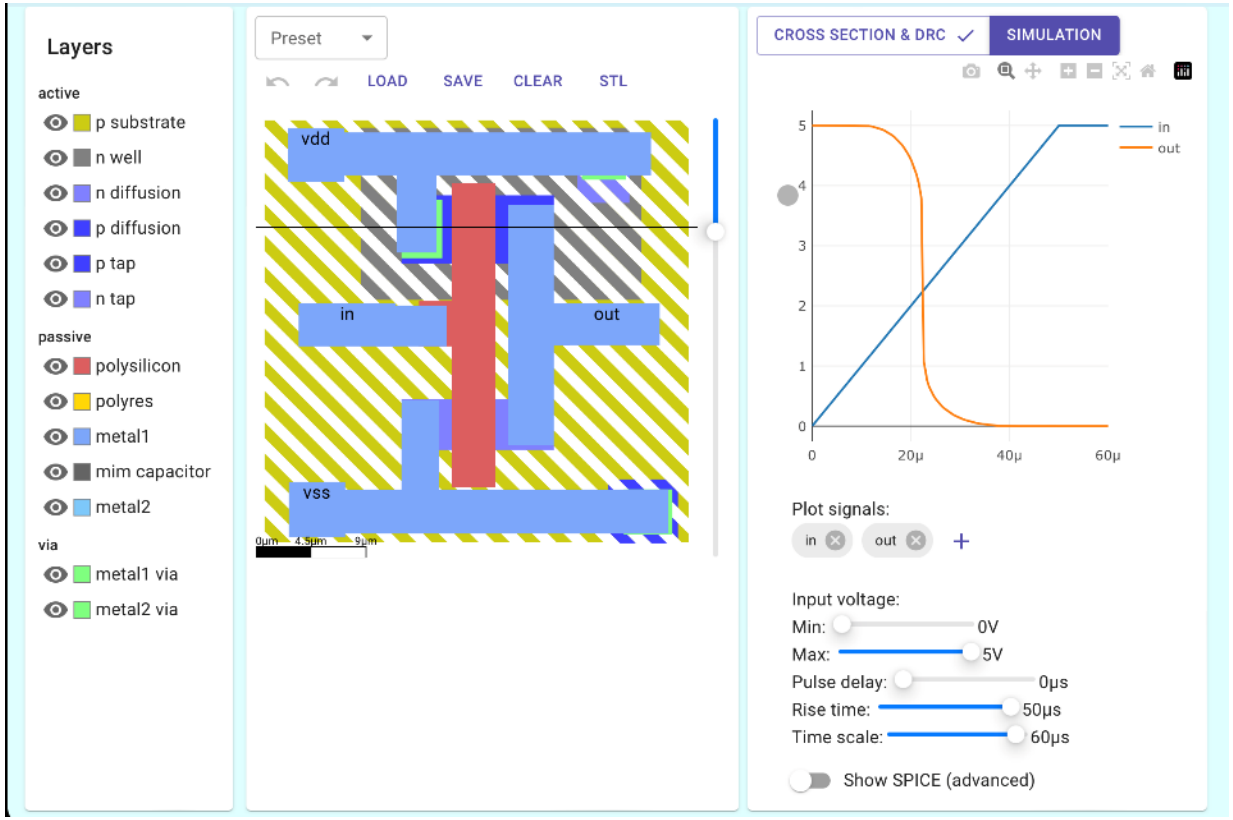
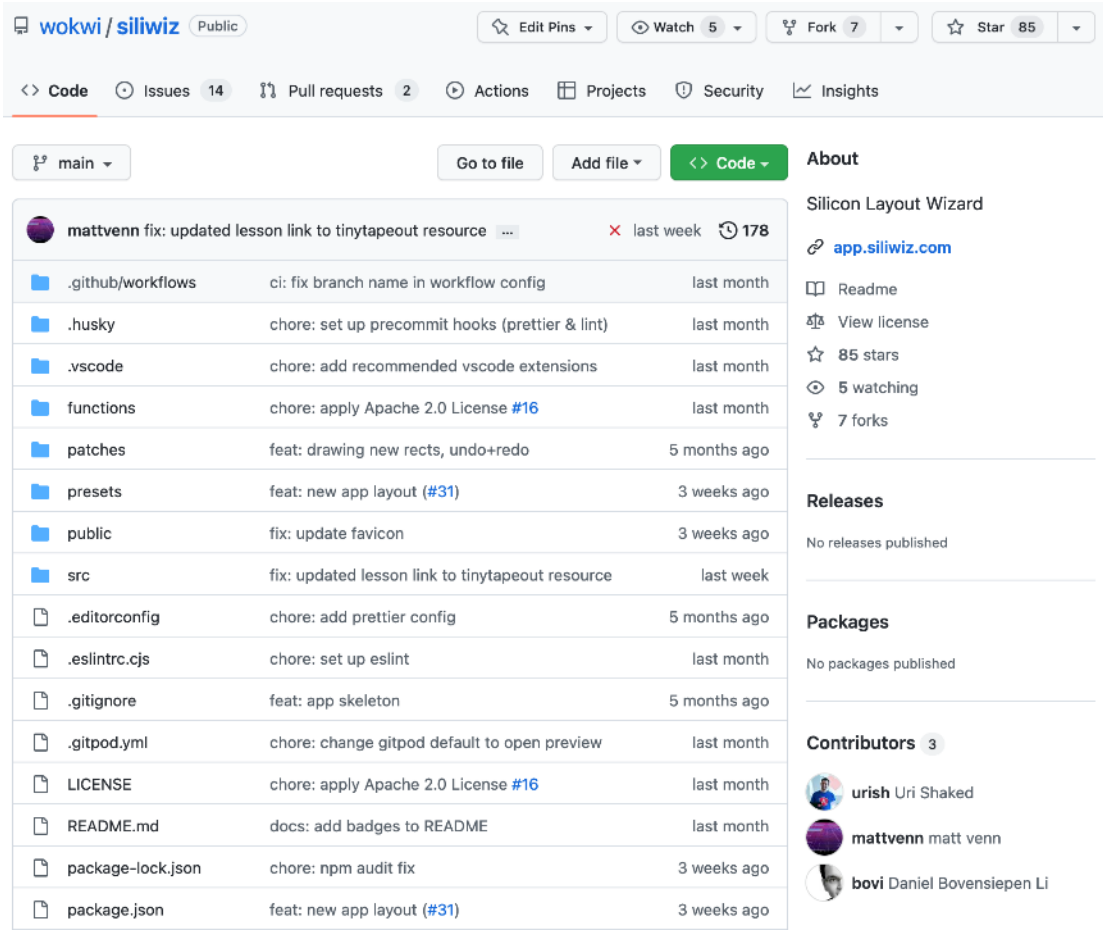
Estimated cost per design if Google doesn't pay anymore

	Multi Project Wafer	Zero2Asic	Tiny Tapeout
parts per design	300	~18	~1
design quantity	1	16	249
design size	10mm²	300µm²	150µm x 170µm
design cost	$9,750.00	$609.38*	$39.16*
design examples	• RISC-V based Arduino • Bitcoin mining accelerator • FPGA • I2C controller	• ChaCha20 accelerator • RGB mixer • A5/1 crypto block • Pong	• temp sensor • CRC calculator • guitar tuner • 12bit PDP8 CPU

* naïve estimation

Understanding semiconductors on a substrate level





https://app.siliwiz.com

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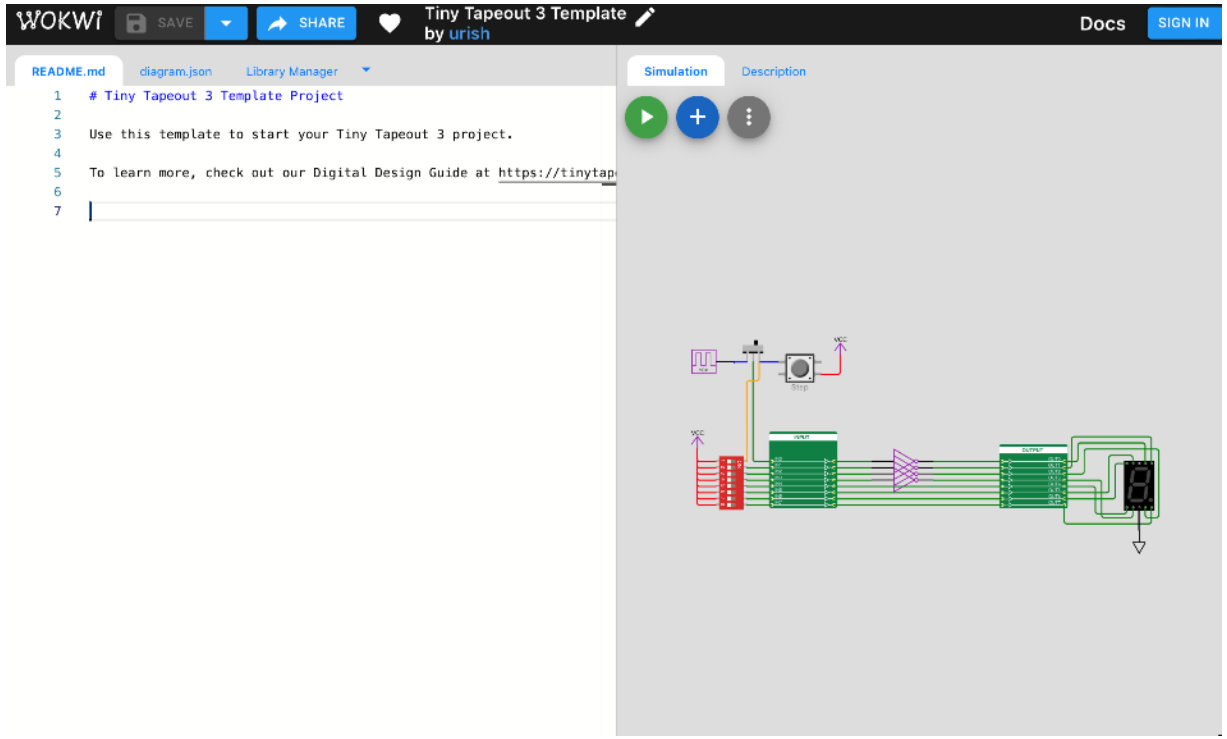
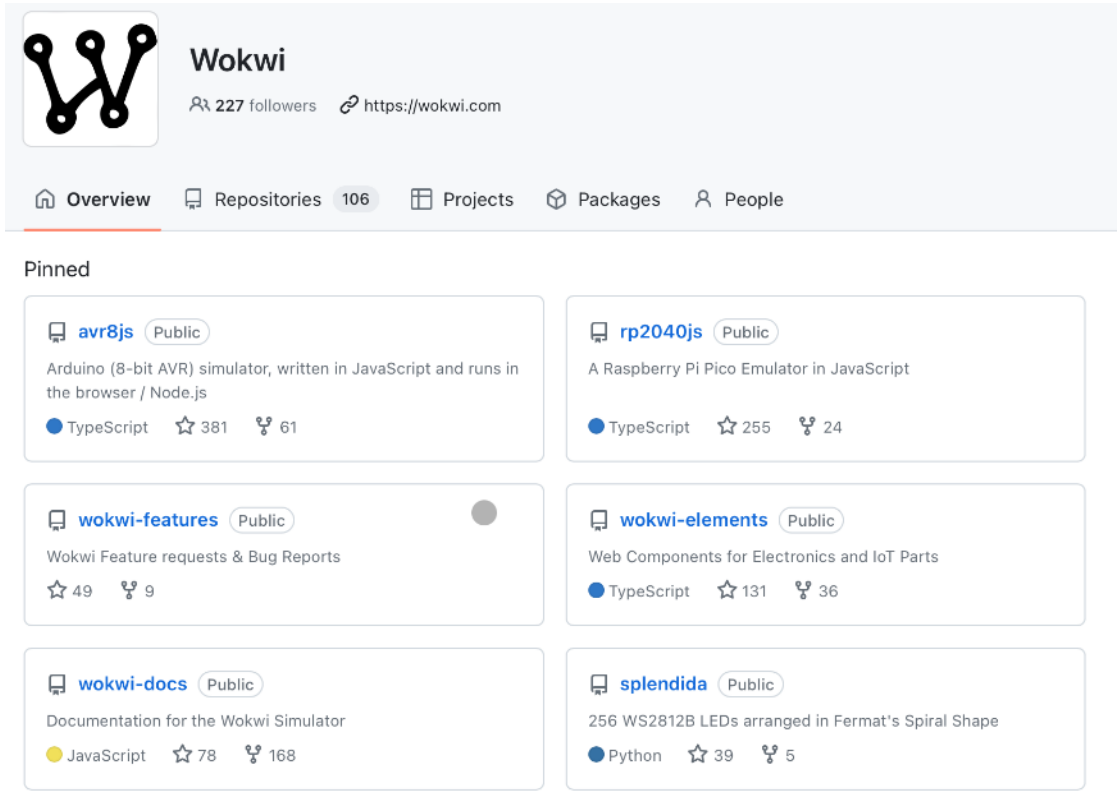
Design electrical circuits in the browser

WOKWI





https://wokwi.com

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“thought-provoking” answers

1) **Do you have basic knowledge how an ASIC is made?**
   I guess somehow…

2) **Do you think an Open Source ASIC is possible today?**
   Looks like it

3) **Do you dare to design your own ASIC?**
   Sure

epilog

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Q&A

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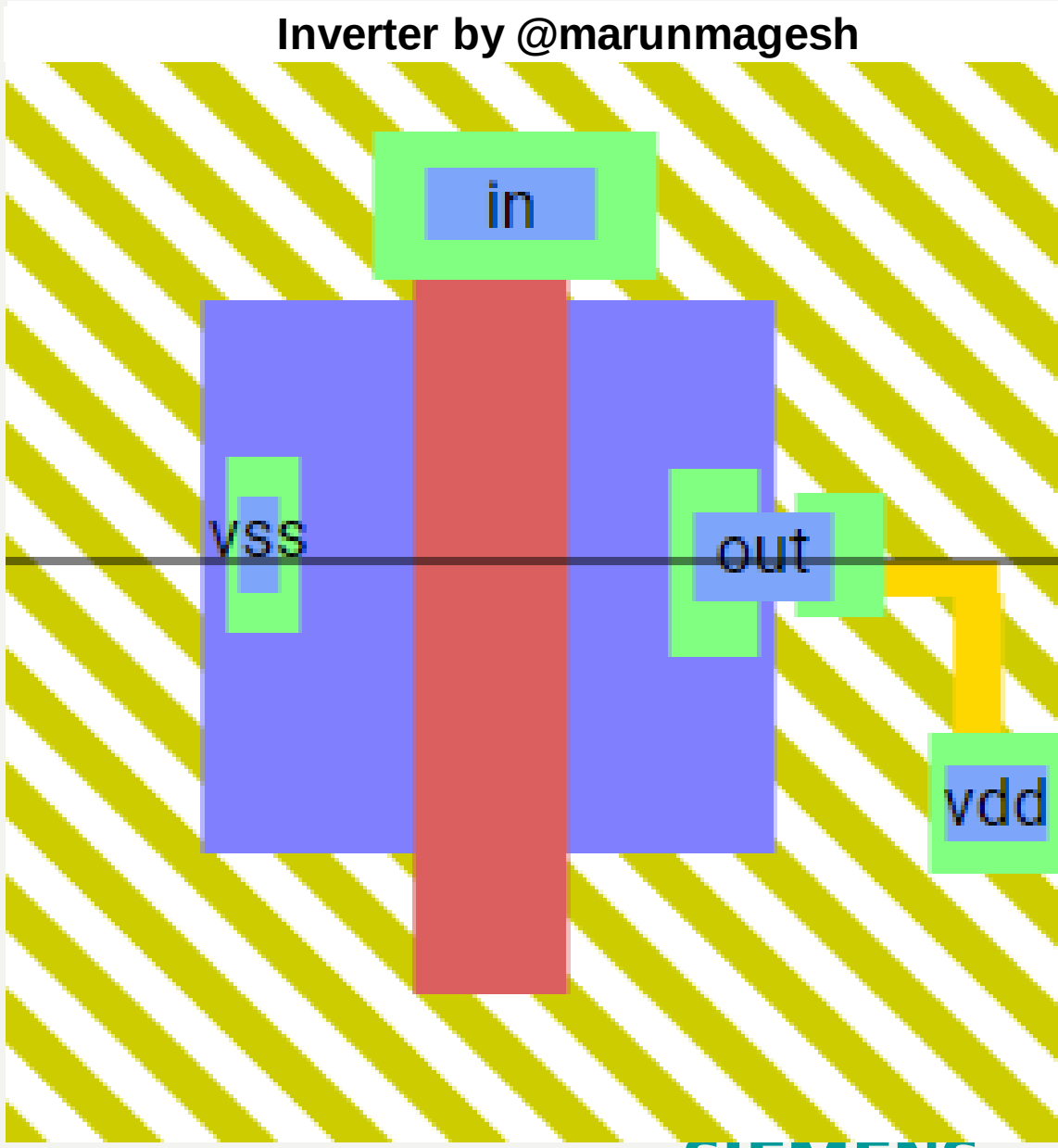

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