# Hardware Development in Open-Source Era

Engineer a smarter future faster



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# Presentation Content

- Composition of Electronic Design Automation (EDA)
  - Software Development Tools
  - Hardware design specification & standards
  - Interface specifications & standards
- Focus on high-end electronic system design
  - Open source for leading edge designs
- Path for standards development and open source to align
- Open source and design in the 2020’s



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# Affiliations

- Siemens Digital Industry Software
  Director of Strategic Business Development

- IEEE Design Automation Standards Committee
  Chair

- IEC TC91 WG13
  Co-Convenor

- Accellera
  Vice Chair

- IEEE SA Open Source Committee (OSCom)
  Member



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# In the beginning

Open Source came early to **E**lectronic **D**esign **A**utomation (EDA)



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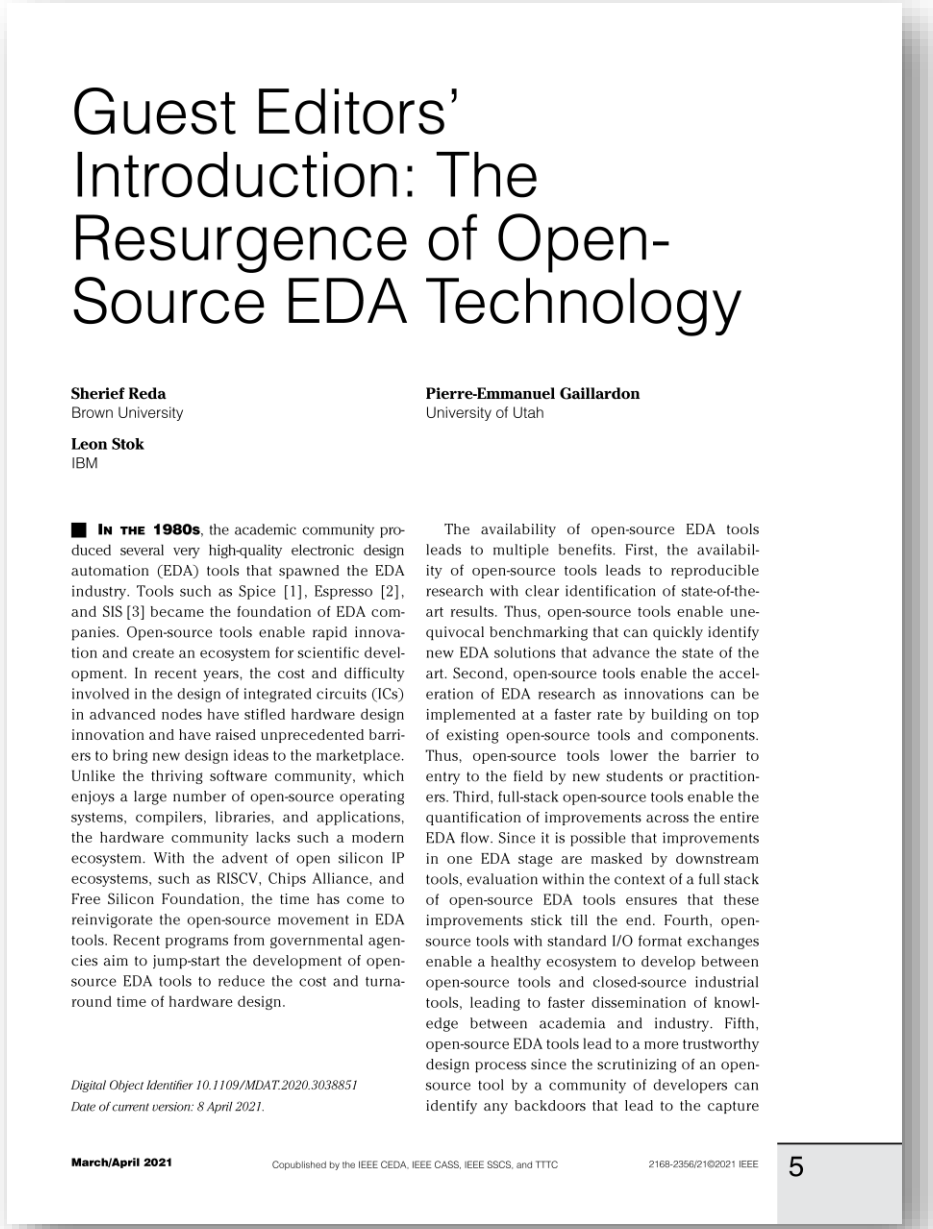
# EDA's History & Future with Open Source

- Public-Domain Software
  - Principles of openness & cooperation from the academic community
- Shareware
  - Limited version of software to promote sales via trial use
  - You like it; you buy it
  - But not open-source
- Freeware
  - Often proprietary, but no monetary cost to the end user
  - Ambiguous set of rights
    - Modification allowed?
    - Redistribution allowed?
    - Reverse engineering acceptable?
- EDA's timeline overlaps with code & file sharing of the 1960's & 70's

- Freeware & Shareware evolved…



Guest Editors' Introduction: The Resurgence of Open-Source EDA Technology

**Sherief Reda**
Brown University

**Pierre-Emmanuel Gaillardon**
University of Utah

**Leon Stok**
IBM

**In the 1980s**, the academic community produced several very high-quality electronic design automation (EDA) tools that spawned the EDA industry. Tools such as Spice [1], Espresso [2], and SIS [3] became the foundation of EDA companies. Open-source tools enable rapid innovation and create an ecosystem for scientific development. In recent years, the cost and difficulty involved in the design of integrated circuits (ICs) in advanced nodes have stifled hardware design innovation and have raised unprecedented barriers to bring new design ideas to the marketplace. Unlike the thriving software community, which enjoys a large number of open-source operating systems, compilers, libraries, and applications, the hardware community lacks such a modern ecosystem. With the advent of open silicon IP ecosystems, such as RISCV, Chips Alliance, and Free Silicon Foundation, the time has come to reinvigorate the open-source movement in EDA tools. Recent programs from governmental agencies aim to jump-start the development of open-source EDA tools to reduce the cost and turnaround time of hardware design.

The availability of open-source EDA tools leads to multiple benefits. First, the availability of open-source tools leads to reproducible research with clear identification of state-of-the-art results. Thus, open-source tools enable unequivocal benchmarking that can quickly identify new EDA solutions that advance the state of the art. Second, open-source tools enable the acceleration of EDA research as innovations can be implemented at a faster rate by building on top of existing open-source tools and components. Thus, open-source tools lower the barrier to entry to the field by new students or practitioners. Third, full-stack open-source tools enable the quantification of improvements across the entire EDA flow. Since it is possible that improvements in one EDA stage are masked by downstream tools, evaluation within the context of a full stack of open-source EDA tools ensures that these improvements stick till the end. Fourth, open-source tools with standard I/O format exchanges enable a healthy ecosystem to develop between open-source tools and closed-source industrial tools, leading to faster dissemination of knowledge between academia and industry. Fifth, open-source EDA tools lead to a more trustworthy design process since the scrutinizing of an open-source tool by a community of developers can identify any backdoors that lead to the capture

*Digital Object Identifier 10.1109/MDAT.2020.3038851*
*Date of current version: 8 April 2021.*



Source: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9398954



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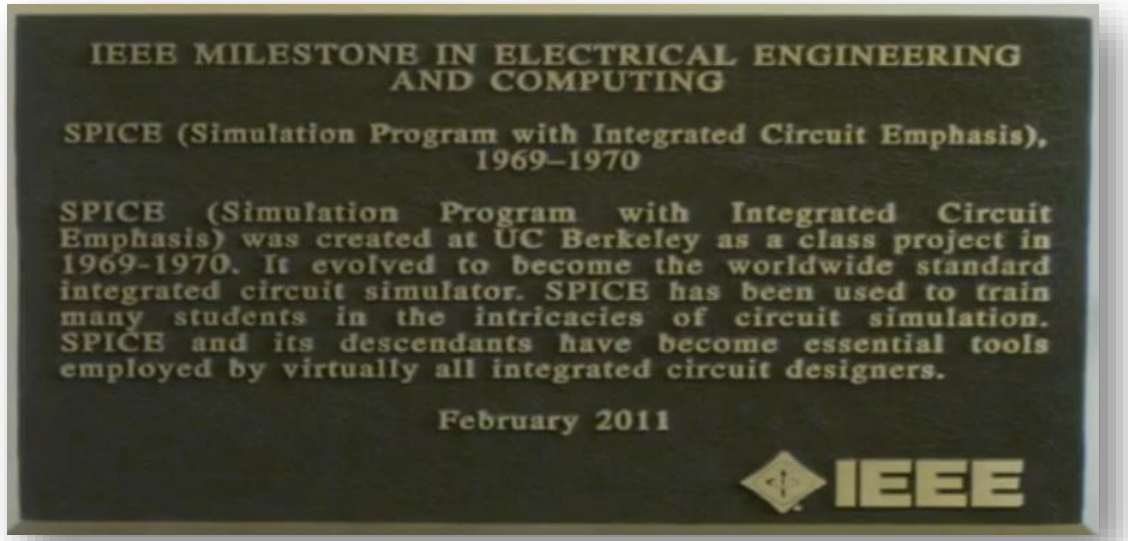
# EDA’s open-source History: SPICE

- Before Digital, Analog was addressed
- Early EDA Shareware includes SPICE
  - UC Berkeley class project under Dr. Ron Rohrer in academic year 1969-1970
  - User interface evolved from punch cards to dumb terminals and commercial workstation implementations
  - Developers made SPICE source code widely available
  - Promoted contributions of more complex device models & analysis capabilities
  - Contribute to its dominance status in subsequent development for both open-source and proprietary circuit simulation software
- IEEE Milestone Plaque
  - Placed at Cory Hall, UC Berkeley




Source: IEEE Council on Electronic Design Automation



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# Spice Celebrates 50th Anniversary

Date of first publication: 4 August 1971

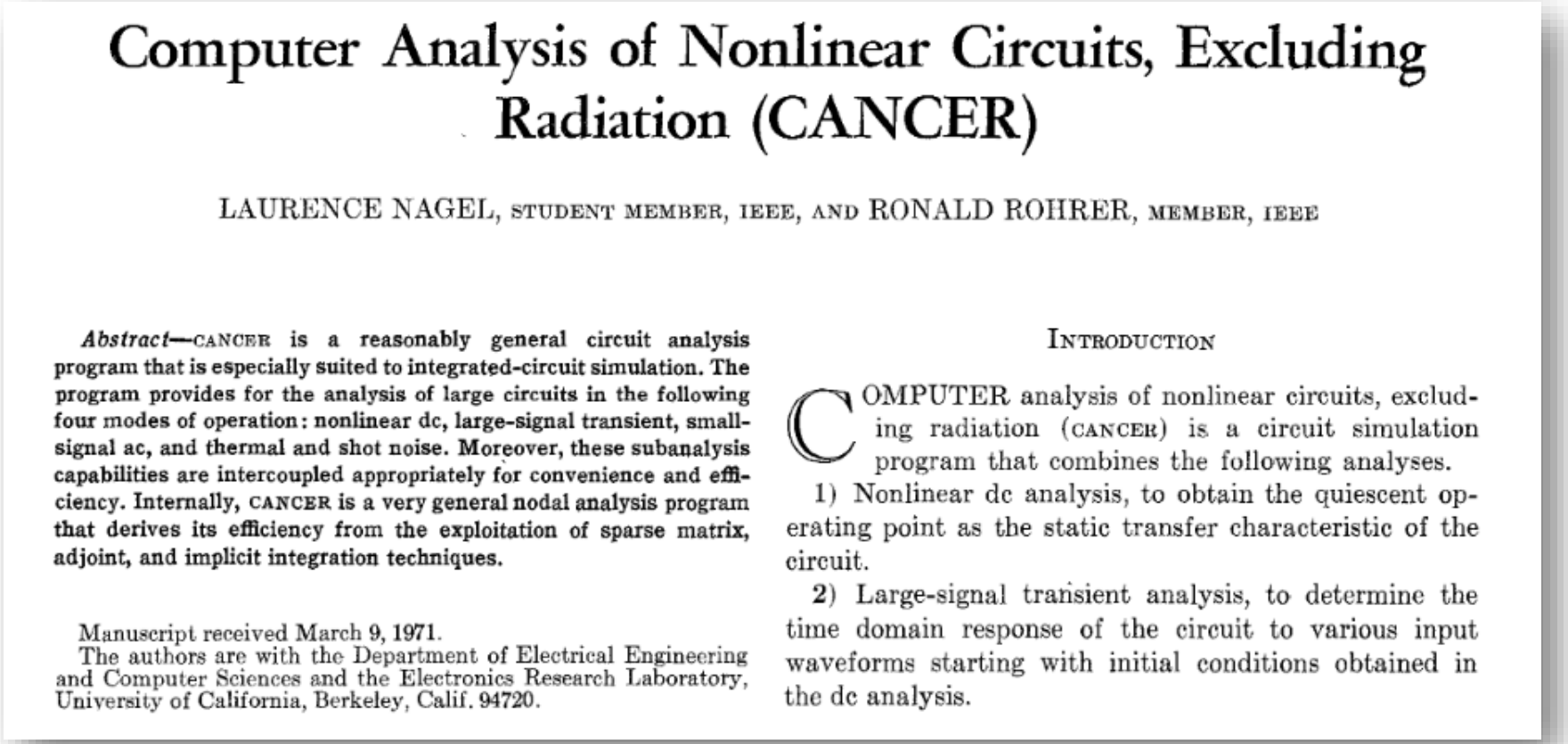
IEEE Journal of Solid-State Circuits

SPICE Evolution

- 1973: SPICE 1
- 1975: SPICE 2
- 1981: HSPICE
- 1984: PSPICE
- 1984: Eldo
- 1986: SPECTRE
- 1989: SPICE 3
- 1993: Last version of SPICE 3 released

New Versions

- Support new models



## Computer Analysis of Nonlinear Circuits, Excluding Radiation (CANCER)

LAURENCE NAGEL, STUDENT MEMBER, IEEE, AND RONALD ROHRER, MEMBER, IEEE

***Abstract*—CANCER is a reasonably general circuit analysis program that is especially suited to integrated-circuit simulation. The program provides for the analysis of large circuits in the following four modes of operation: nonlinear dc, large-signal transient, small-signal ac, and thermal and shot noise. Moreover, these subanalysis capabilities are intercoupled appropriately for convenience and efficiency. Internally, CANCER is a very general nodal analysis program that derives its efficiency from the exploitation of sparse matrix, adjoint, and implicit integration techniques.**

Manuscript received March 9, 1971.
The authors are with the Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, University of California, Berkeley, Calif. 94720.

### INTRODUCTION

COMPUTER analysis of nonlinear circuits, excluding radiation (CANCER) is a circuit simulation program that combines the following analyses.

1) Nonlinear dc analysis, to obtain the quiescent operating point as the static transfer characteristic of the circuit.

2) Large-signal transient analysis, to determine the time domain response of the circuit to various input waveforms starting with initial conditions obtained in the dc analysis.

Source: IEEE Electronic Library
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# Transistor-Level Simulation

- The first “open-source” EDA Standard
  - CANCER
  - Ron Roher

- SPICE – Simulation Program with Integrated Circuit Emphasis
  - L.W. Nagel and D.O. Pederson
  - Presented April 12, 1973




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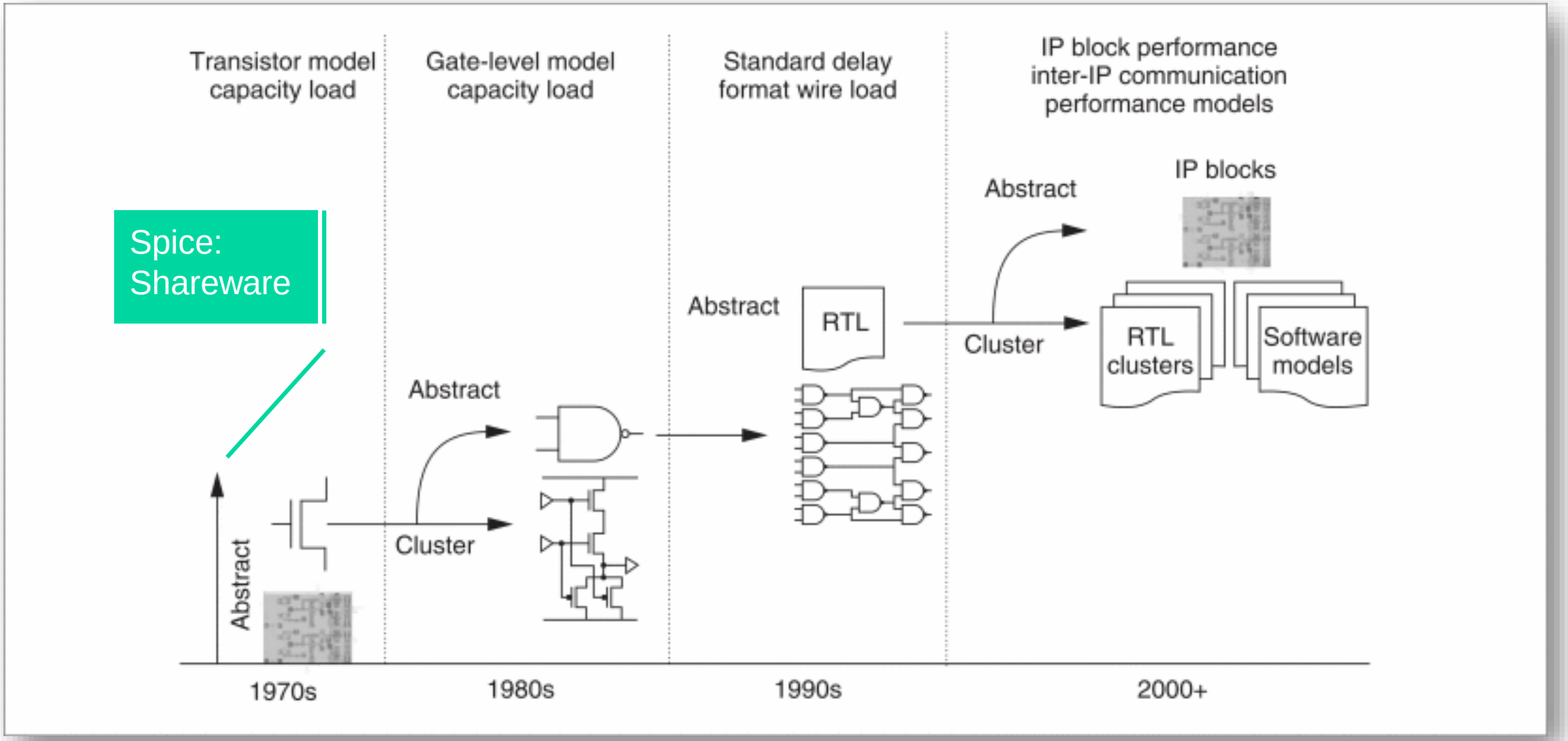
# Productivity Through Abstraction
# Digital Design View

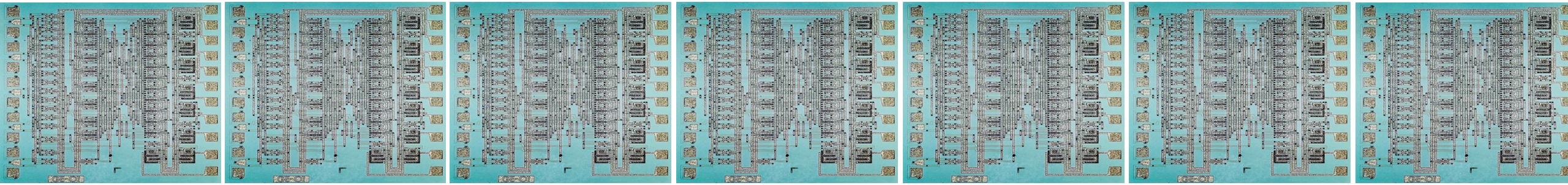



Source: IEEE Design & Test of Computers
https://ieeexplore.ieee.org/document/1246165

# Large Scale Integration (LSI) Evolves to VLSI

SSI/MSI design and verify

- Manual design and layout
- Fabricate it
- Test it
- Re-design it
- Repeat





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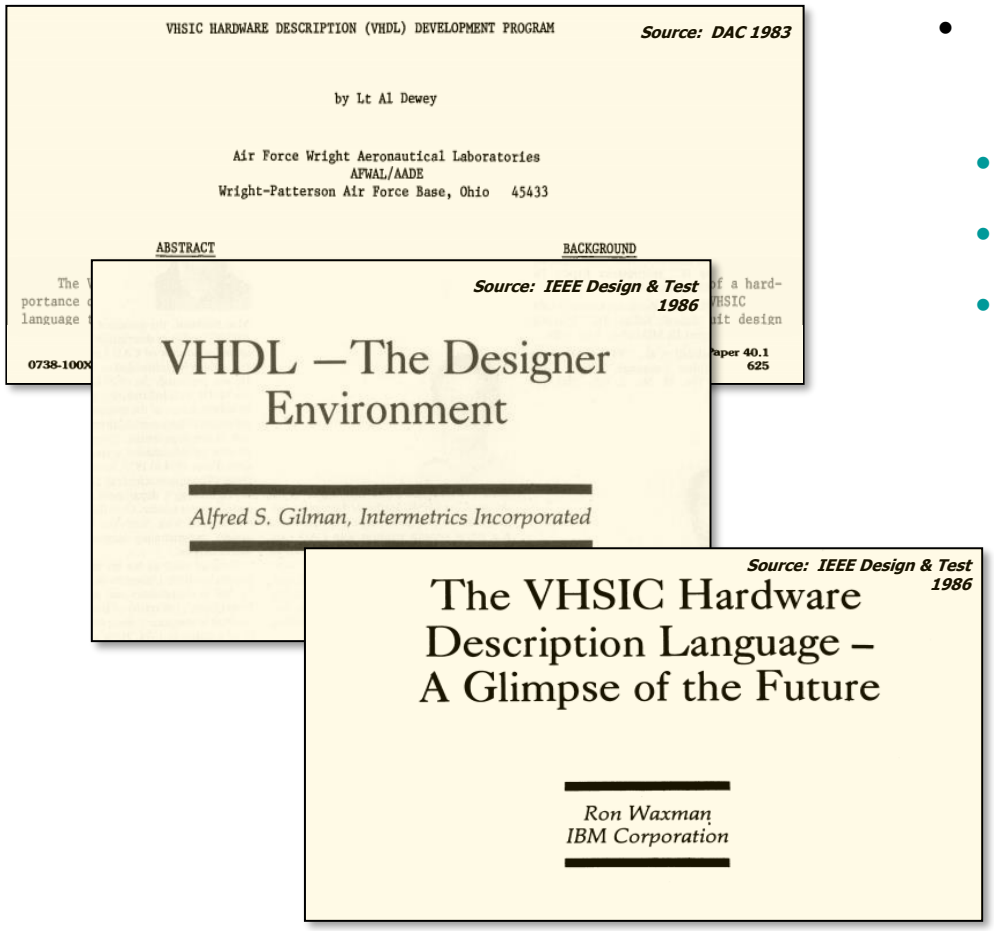
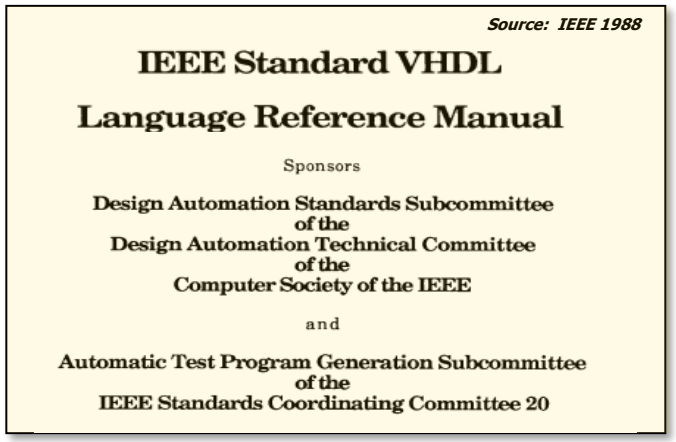
# VHSIC Hardware Description Language (VHDL)




- IBM, Texas Instruments & Intermetrics awarded contract – 1983
  - VHSIC Hardware Description Language
  - VHDL 7.2 release in 1985
  - VHDL became IEEE Std. 1076™-1987



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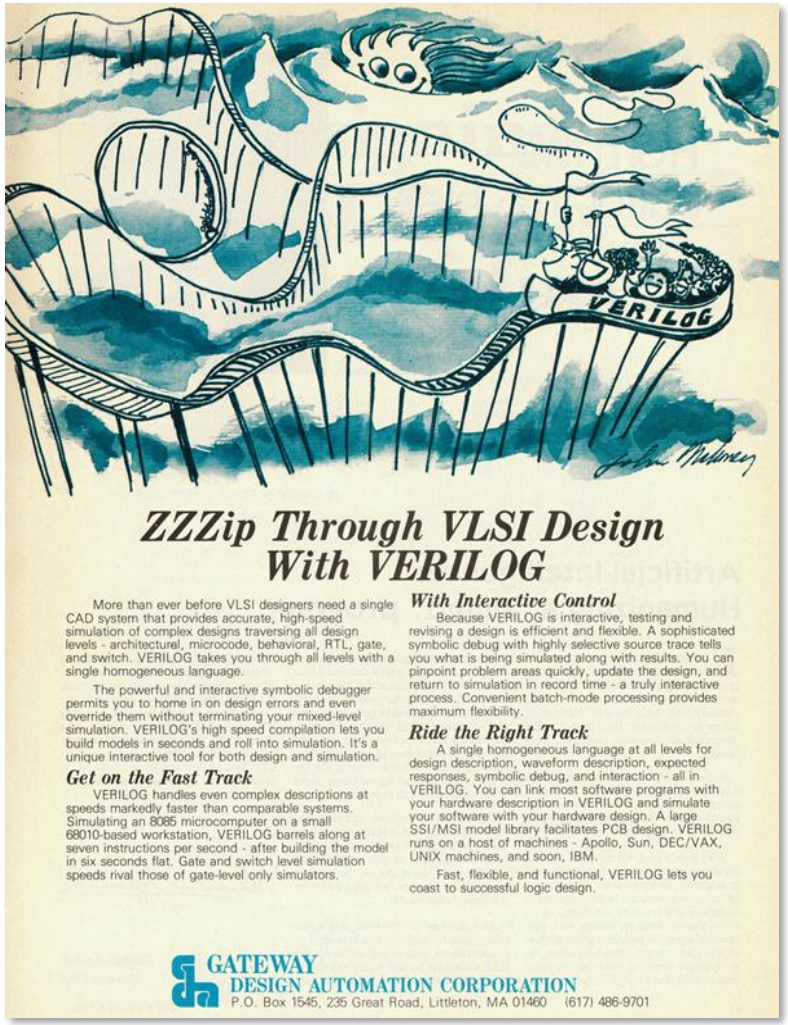
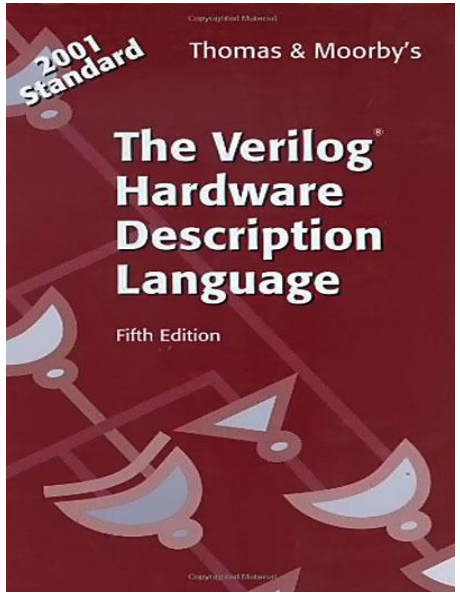
# Verilog Hardware Description Language




Source: IEEE Design & Test of Computers, August 1985

- Gateway Design Automation – 1985
  - Verilog HDL created by Phil Moorby in 1984
  - Acquired by Cadence in 1989
  - Verilog became IEEE Std. 1364™-1995



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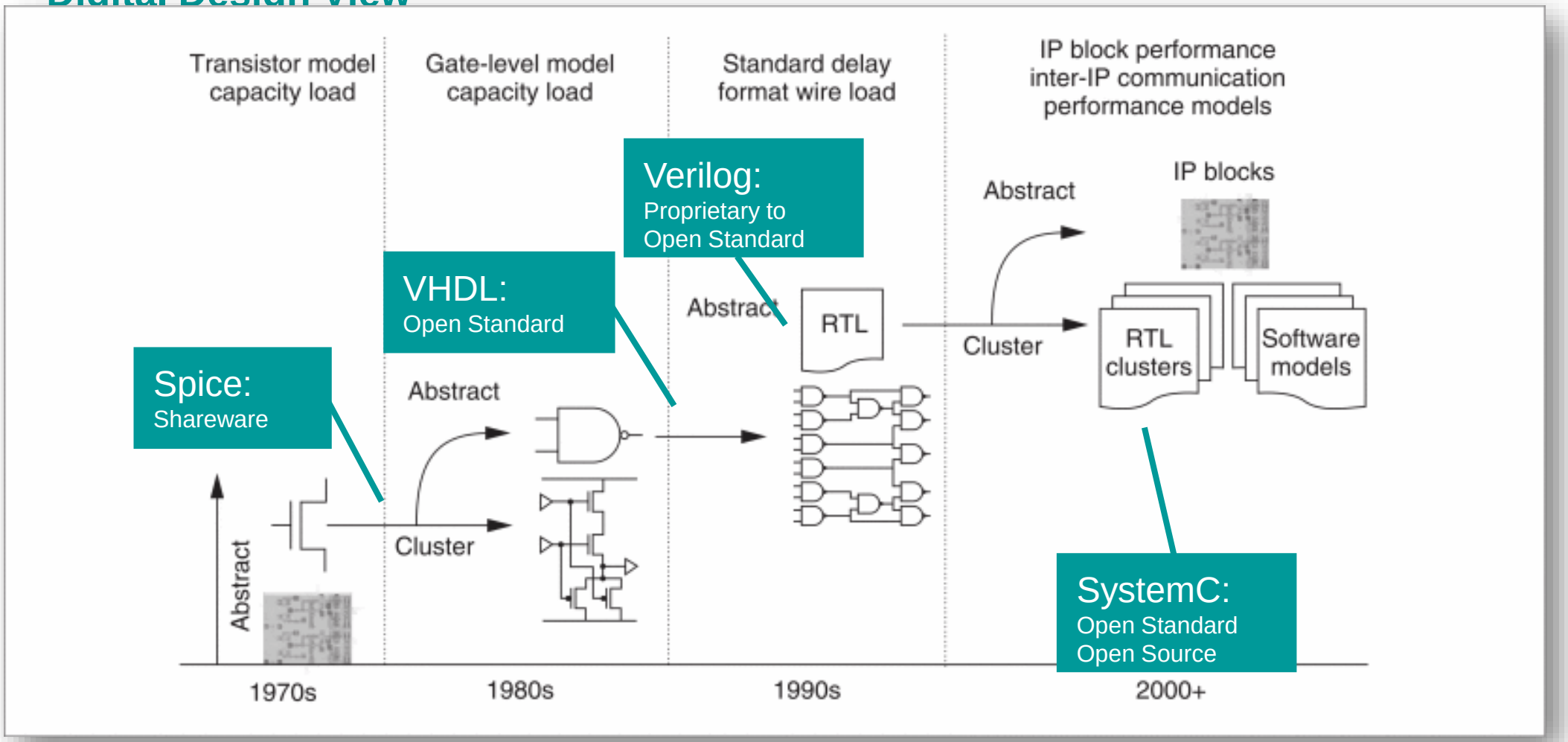
# Productivity Through Abstraction
## Digital Design View




Source: IEEE Design & Test of Computers
https://ieeexplore.ieee.org/document/1246165



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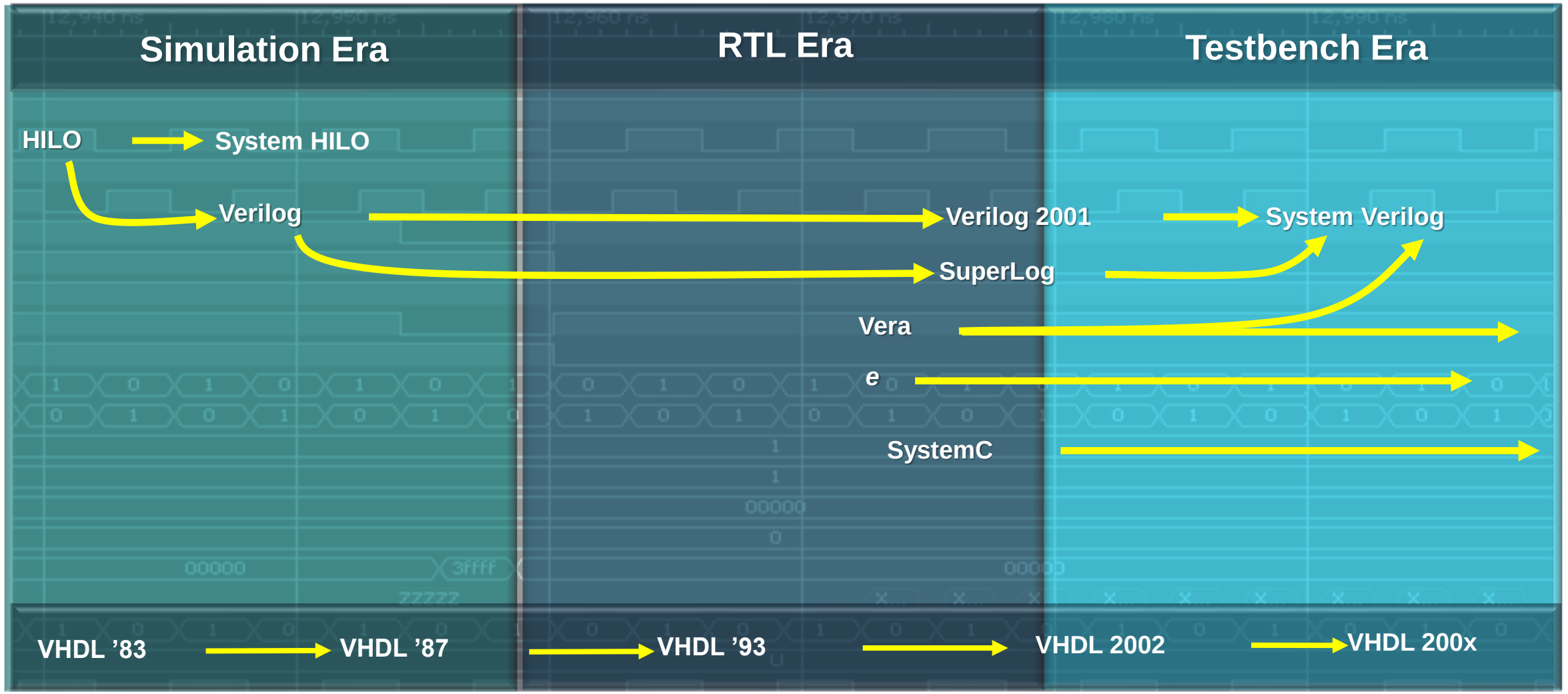
# Language Evolution
# Proprietary to Open Standard to Open Source



# Pervasive use of Open-Source in Electronic Design Automation

Open-Source is here to stay

IEEE Computer Society Design Automation Standards Committee

- Many other DASC standards embrace open-source
- Opportunity to migrate to IEEE SA Open

Industry

- IEEE SA Open Permissive License supports Industry adoption
- Tool interoperability
- Technology differentiation

Academia

- Accelerate EDA research and innovation
- Reproducible research

Governments

- EU Study – Insights on quantitative impacts of Open Source [Dr. Knut Blind]
  - a 10% increase in the number of contributors would increase EU GDP by 0.6%, i.e. €95 billion per year
  - Study: https://openforumeurope.org/wp-content/uploads/2020/11/OFE_Fraunhofer_OS_impact_study_5_Nov.pdf

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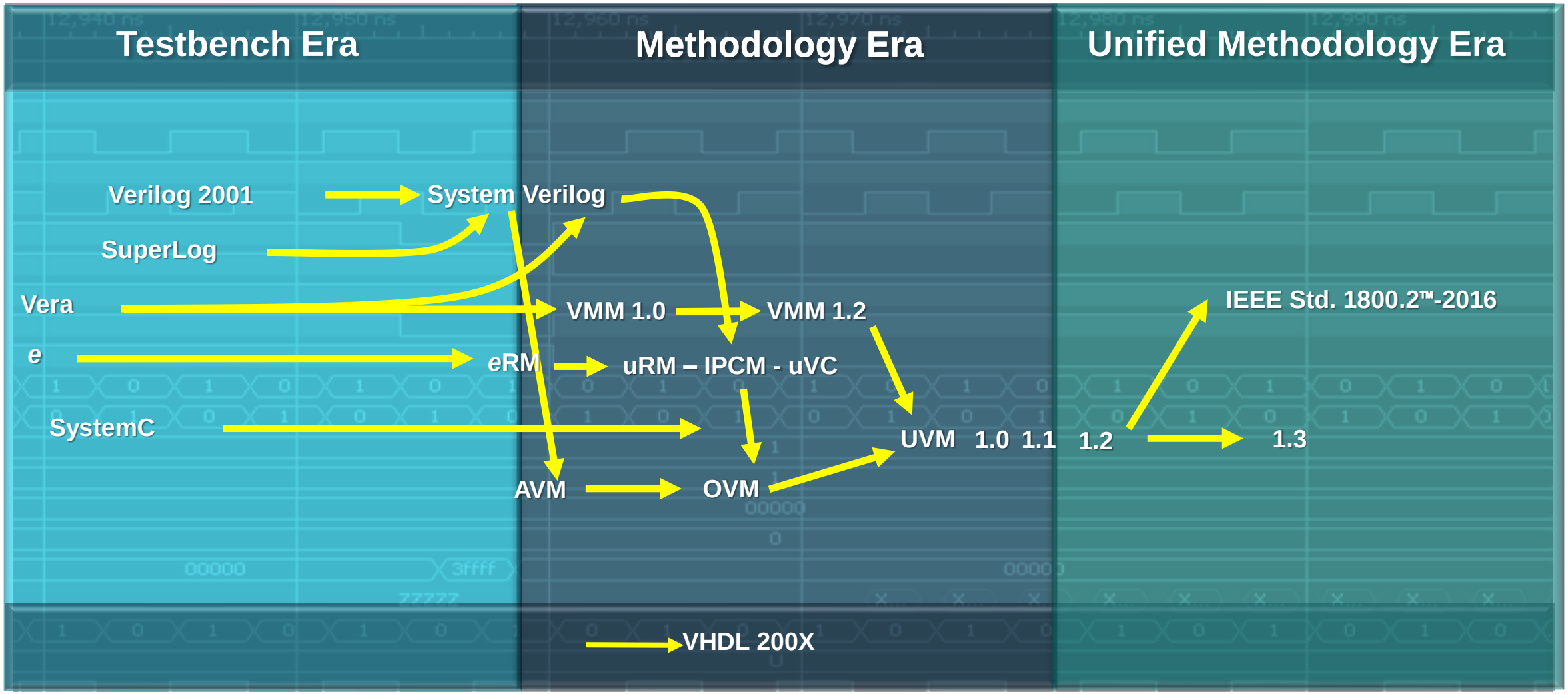
# Methodology Evolution
# Proprietary to Open Source with Open Standard



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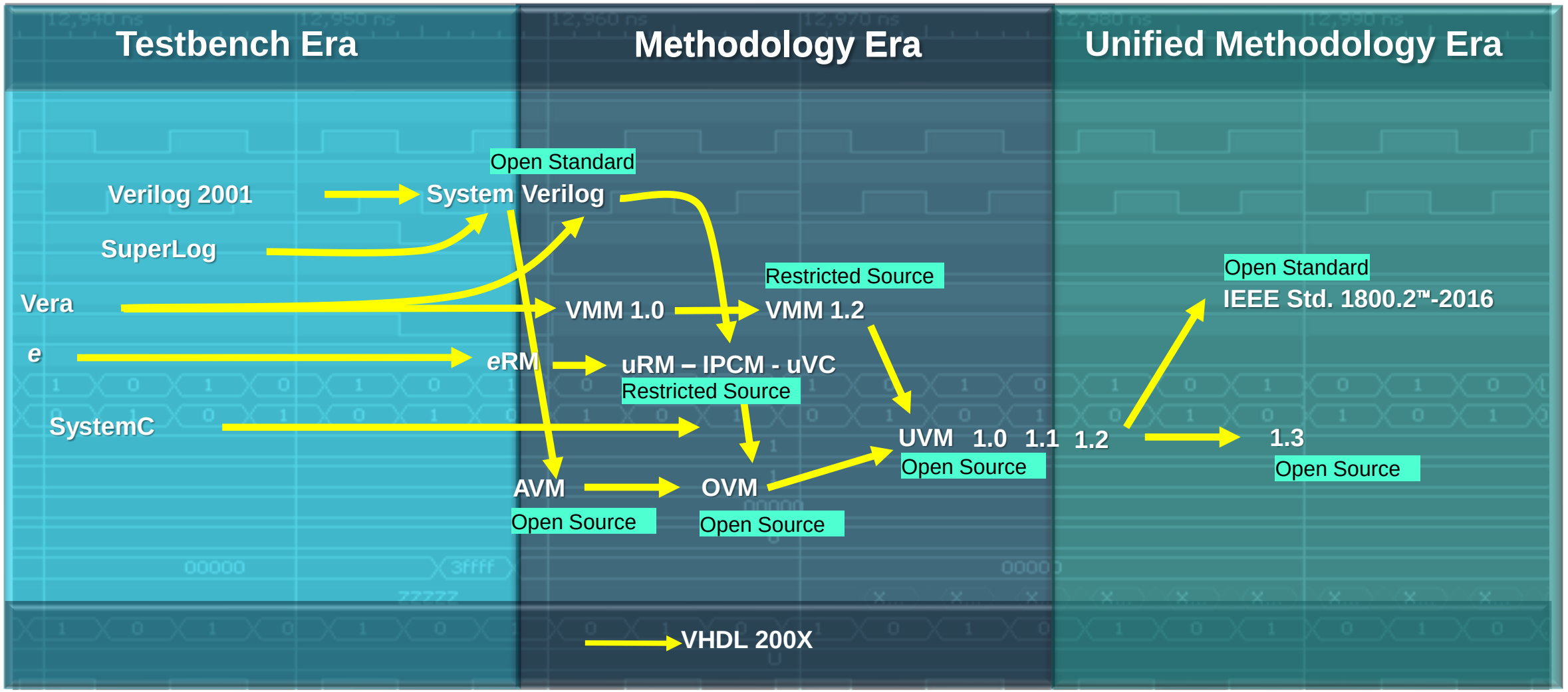
# Methodology Evolution
# Proprietary to Open Source with Open Standard



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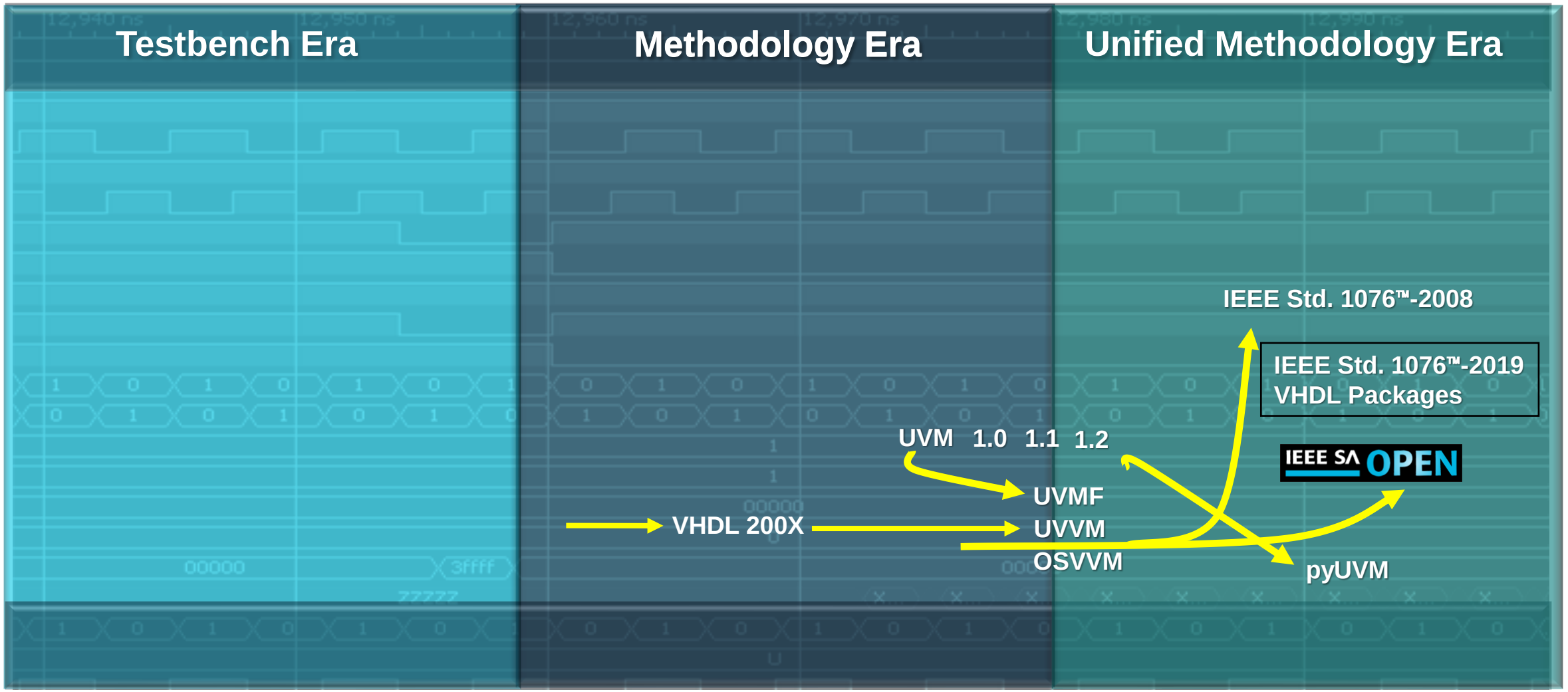
# Methodology Evolution
# VHDL Drives IEEE SA Open



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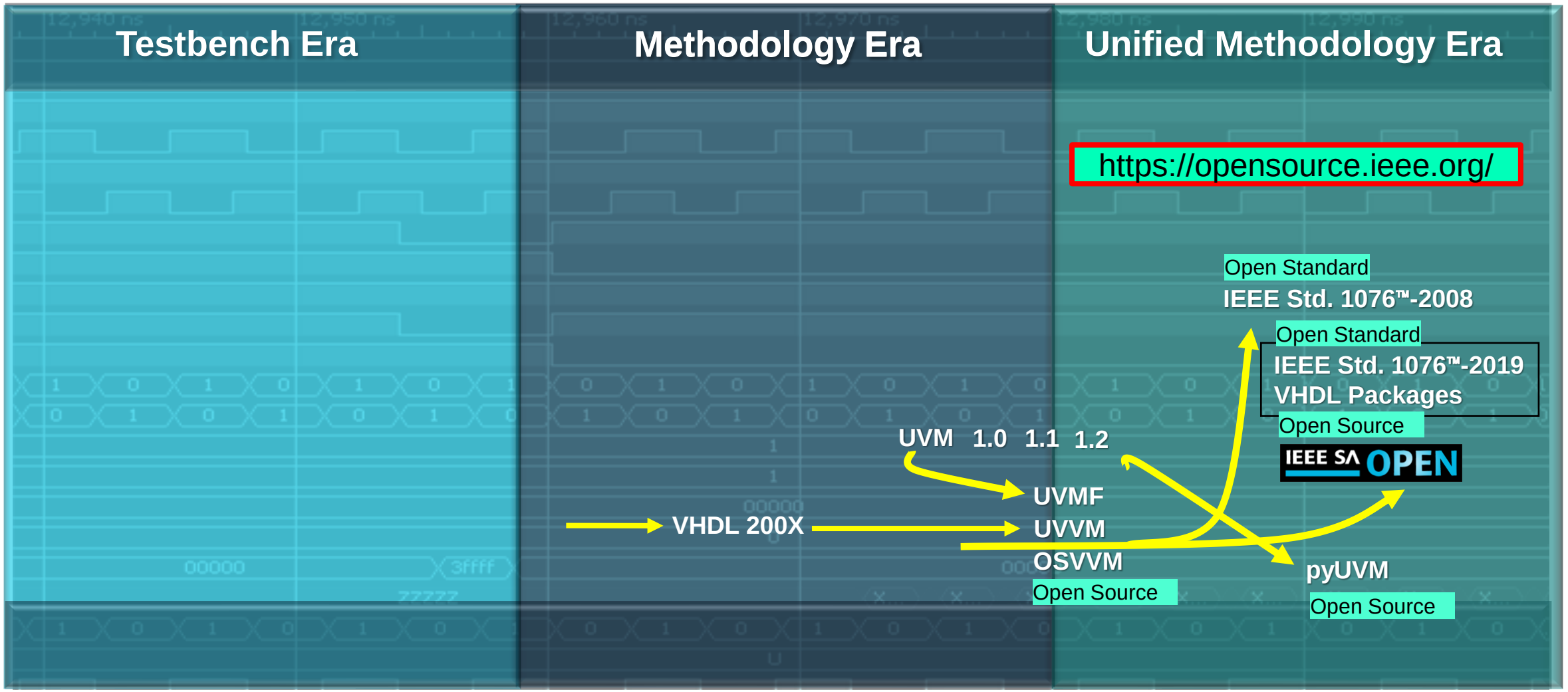
# Methodology Evolution
# Proprietary to Open Source with Open Standard



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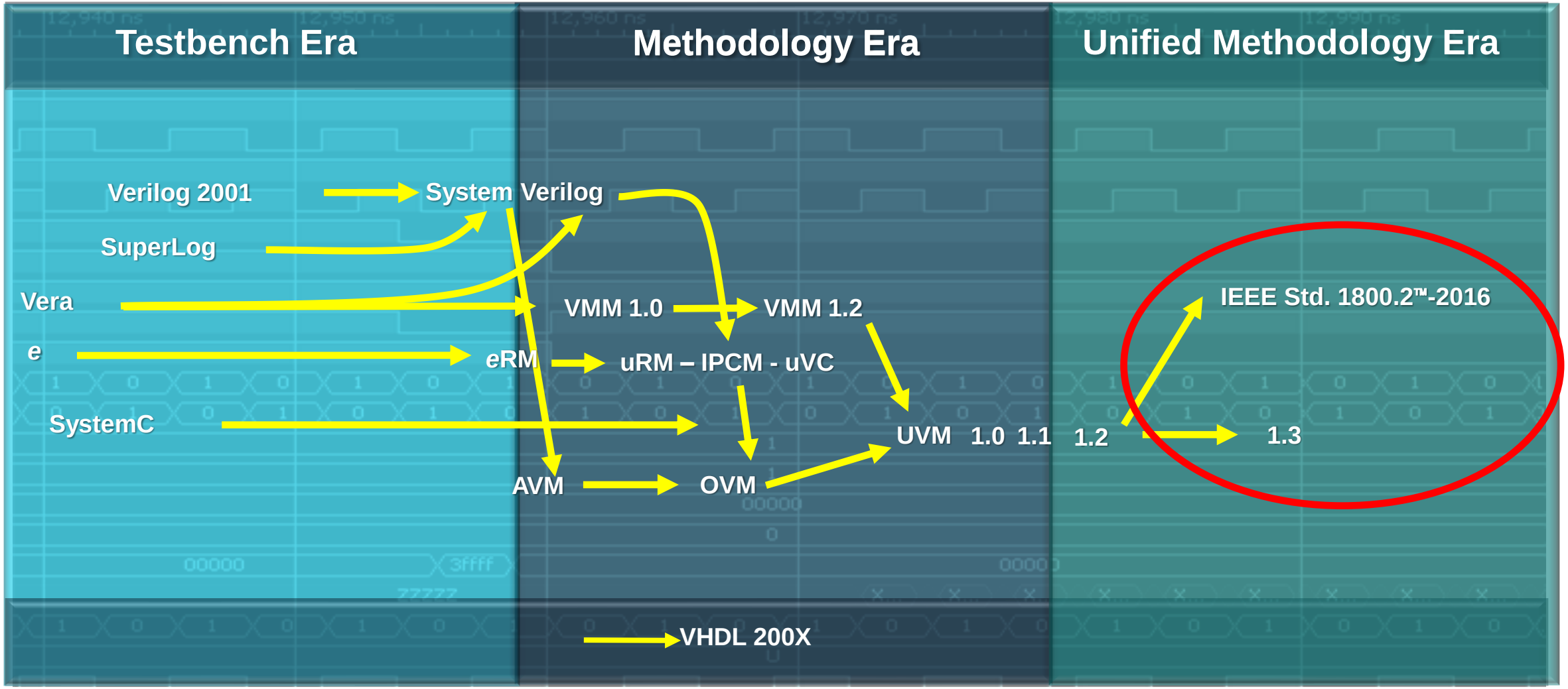
# Methodology Evolution
# SystemVerilog Opportunity under IEEE SA Open



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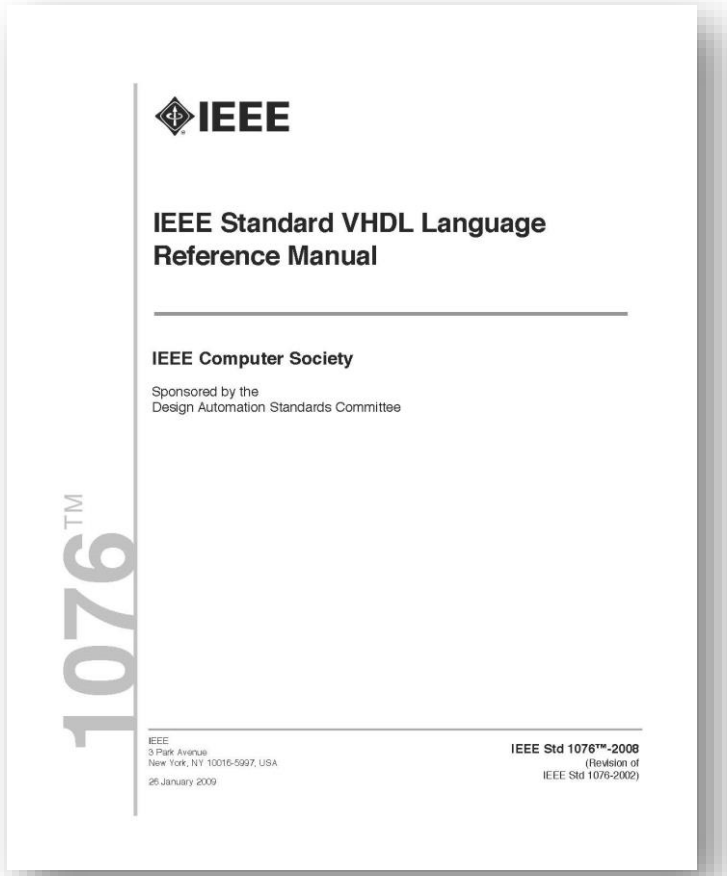
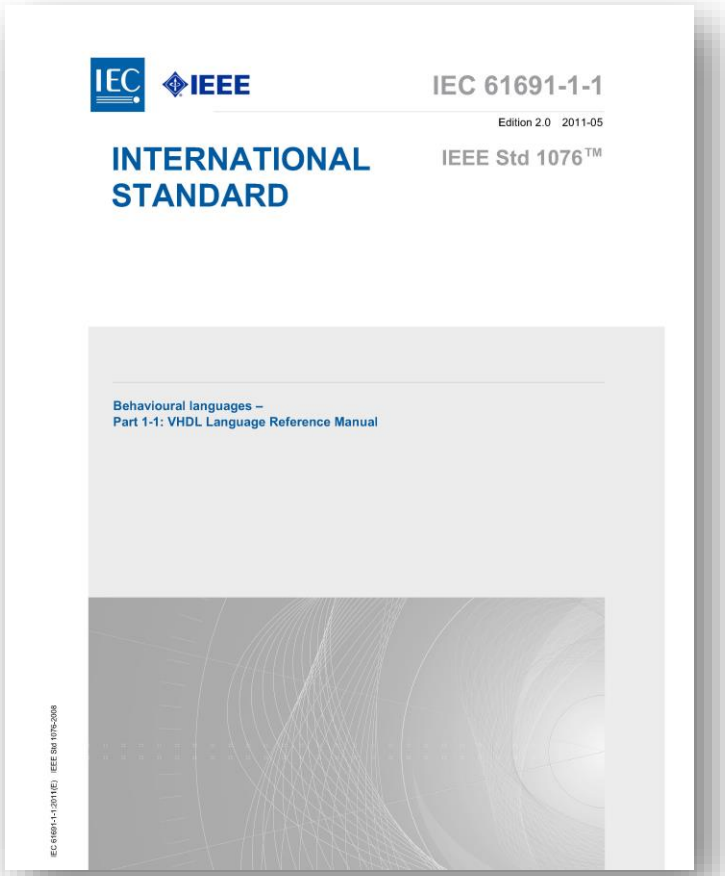
# VHDL: Open Source joins Open Standard




- VHDL Standard “package code” embedded in standard
- Source code also available from IEEE at documented website
- Copyright holder ambiguous
  - IEEE?
  - IEC?
  - Acknowledged contributors?

- Move to Apache license
- IEEE SA Open
  - https://opensource.ieee.org/vasg/Packages/-/tree/1076-2019



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# Language & Methodology Adoption Trends

What is the traction?



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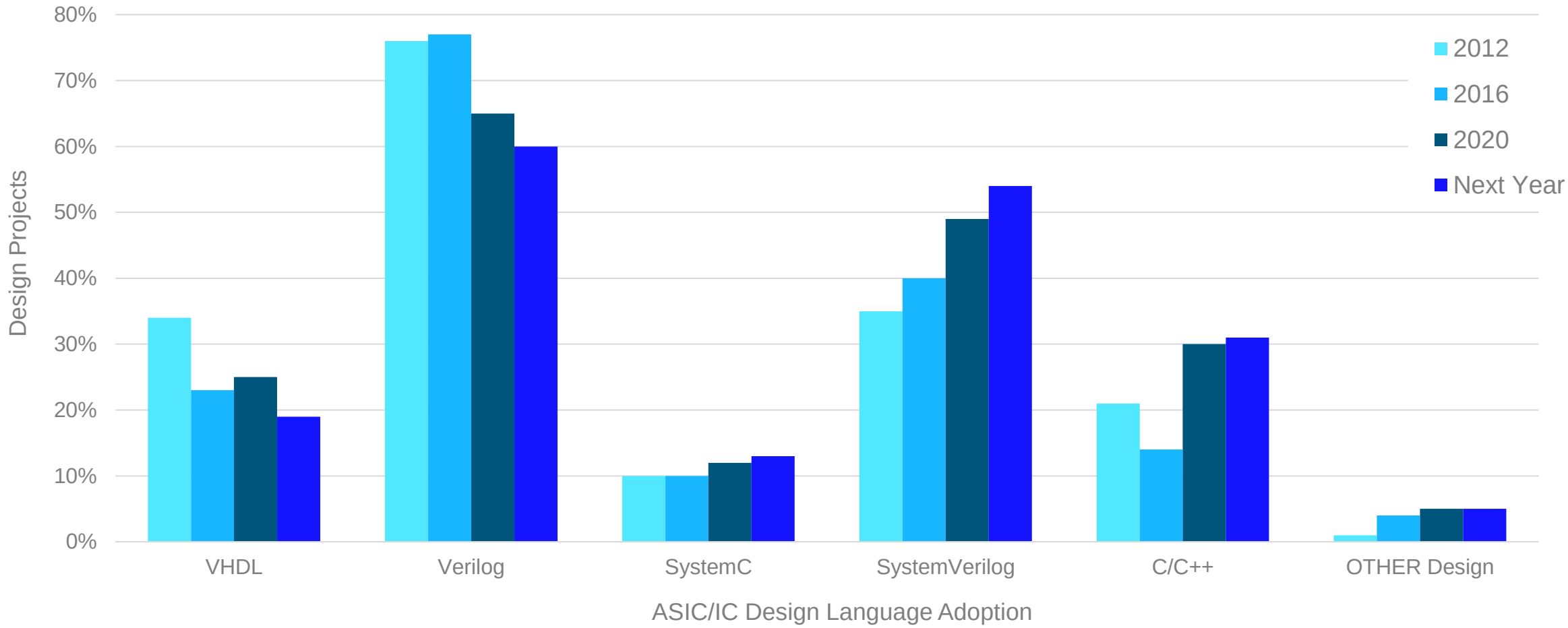
# ASIC/IC Design Language Adoption




*Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study*

** Multiple answers possible



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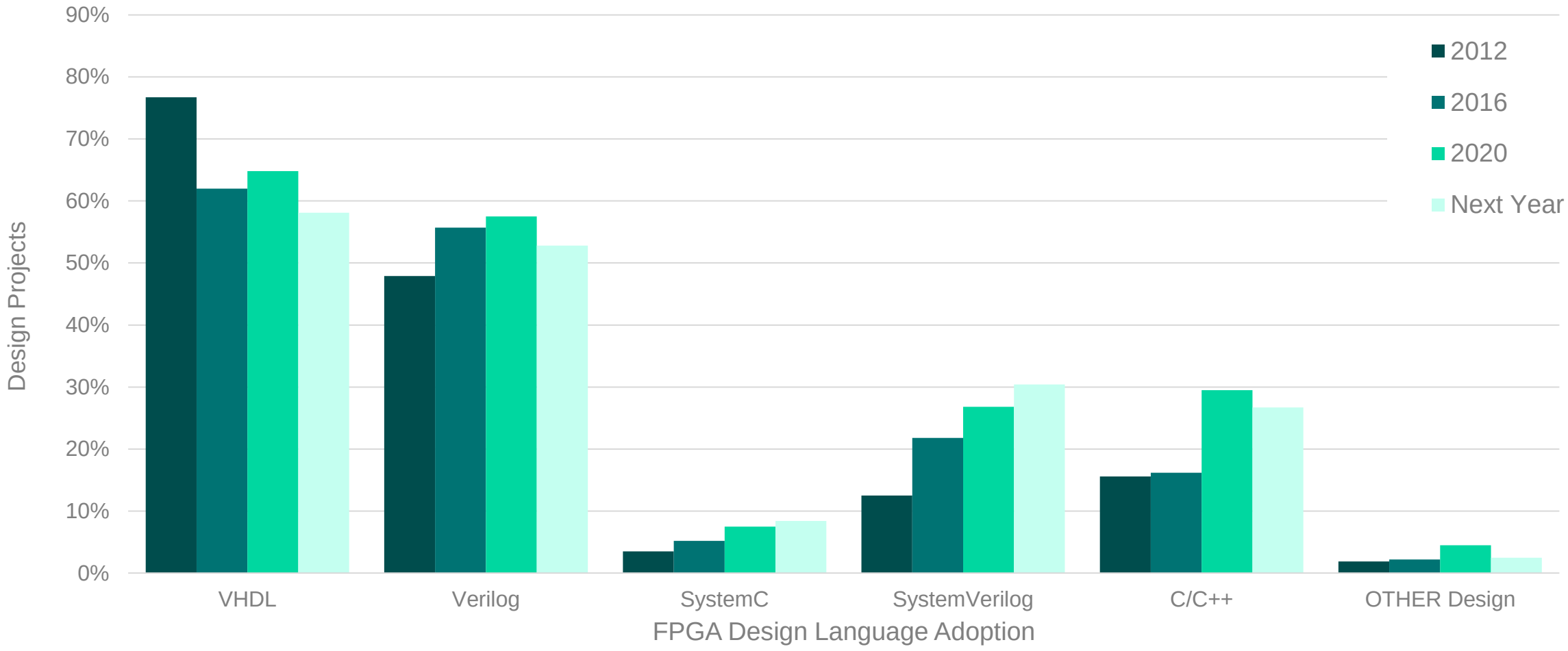
# FPGA Design Language Adoption Next Twelve Months

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** Multiple answers possible



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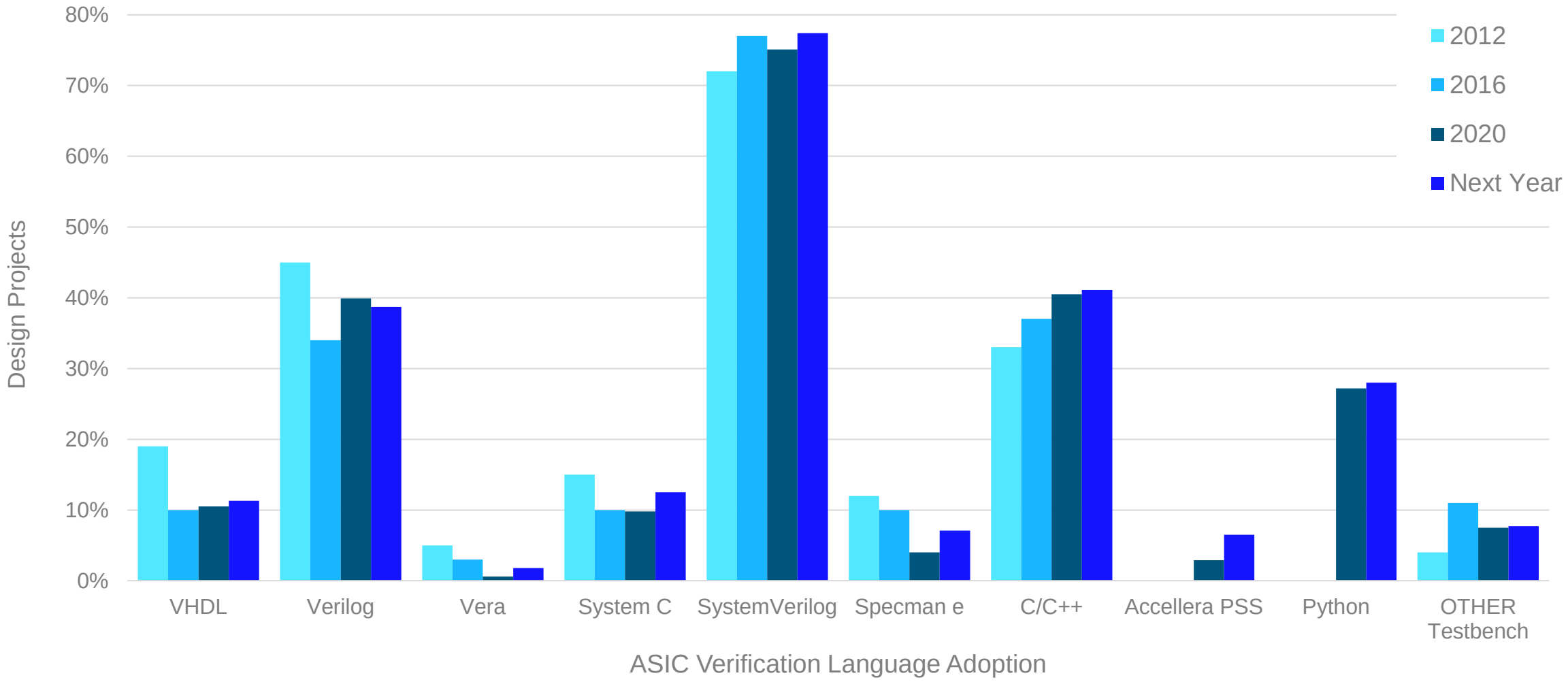
# ASIC/IC Verification Language Adoption Next Twelve Months

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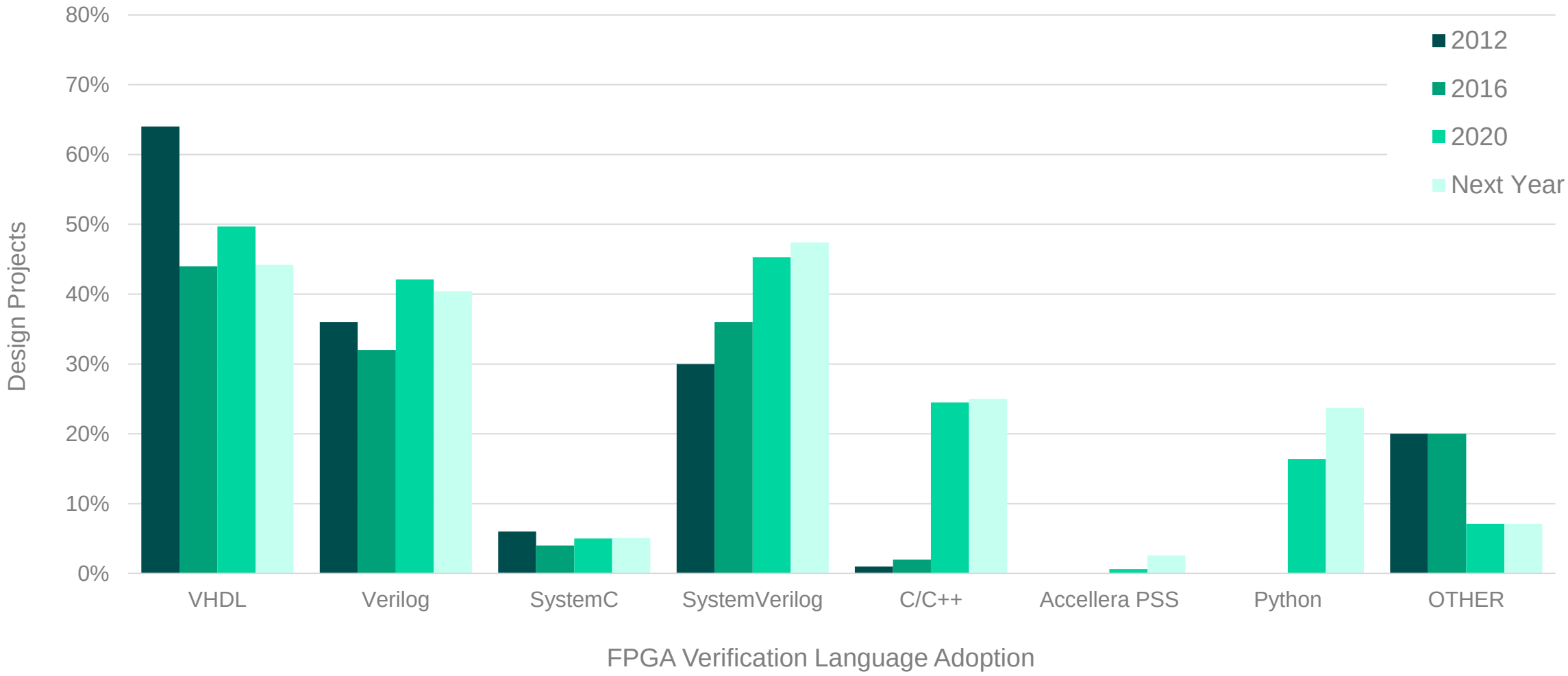


*Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study*

** Multiple answers possible



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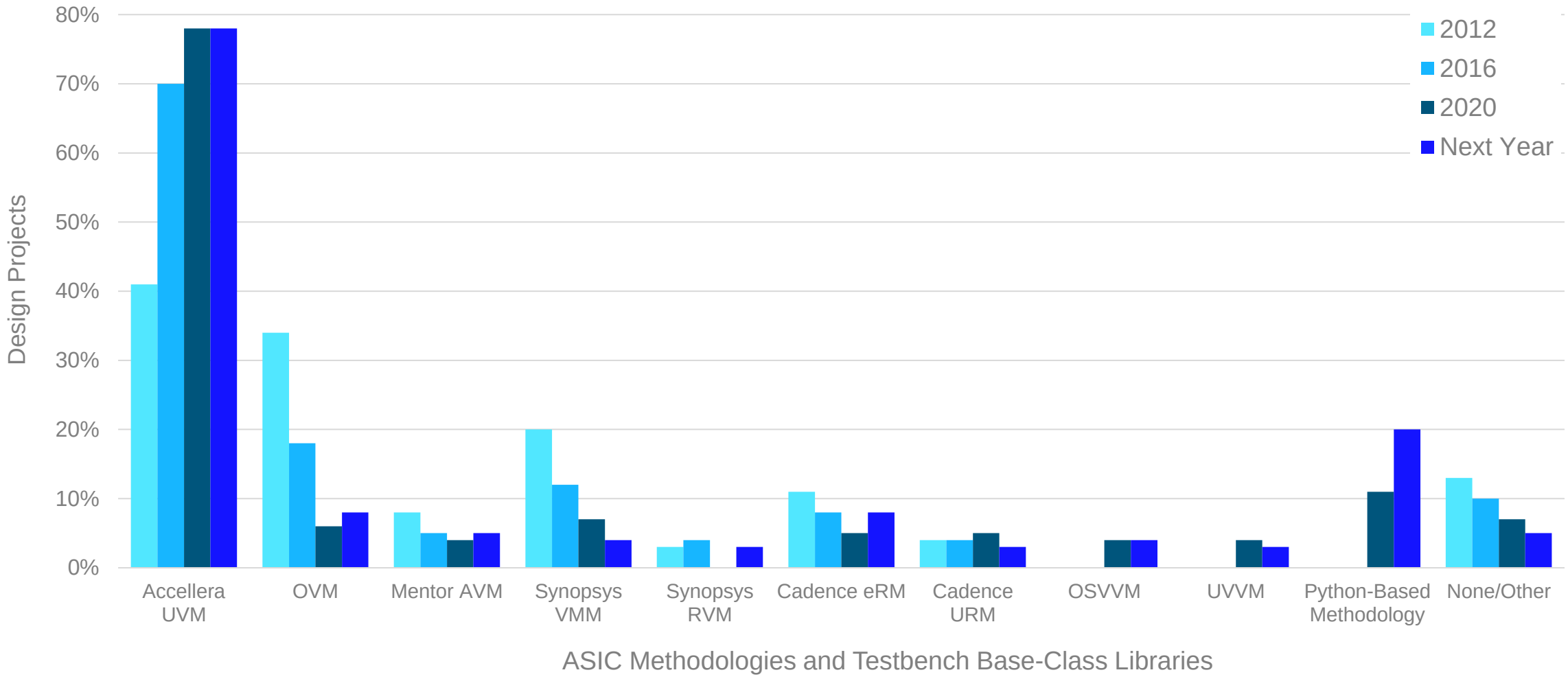
# ASIC Methodologies and Testbench Base-Class Libraries




*Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study*

** Multiple answers possible



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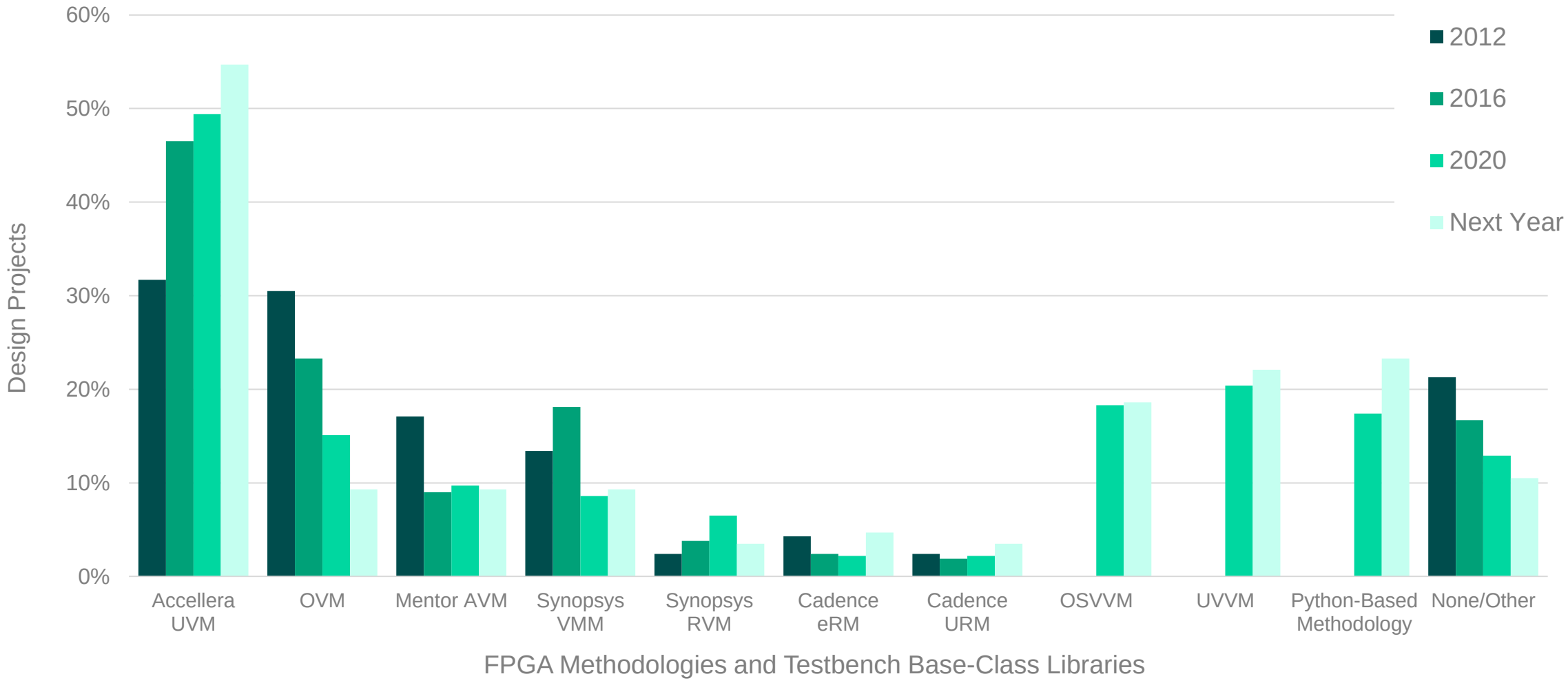
# FPGA Methodologies and Testbench Base-Class Libraries




*Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study*

** Multiple answers possible



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# Systems in the 2020’s

## Open Source Impact



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Software is eating the world…

…demanding evermore advanced hardware.

## AI/ML is making it all smarter, faster

https://future.a16z.com/software-is-eating-the-world/
…VC, Marc Andreesen. Originally published in The Wall Street Journal on August 20, 2011.



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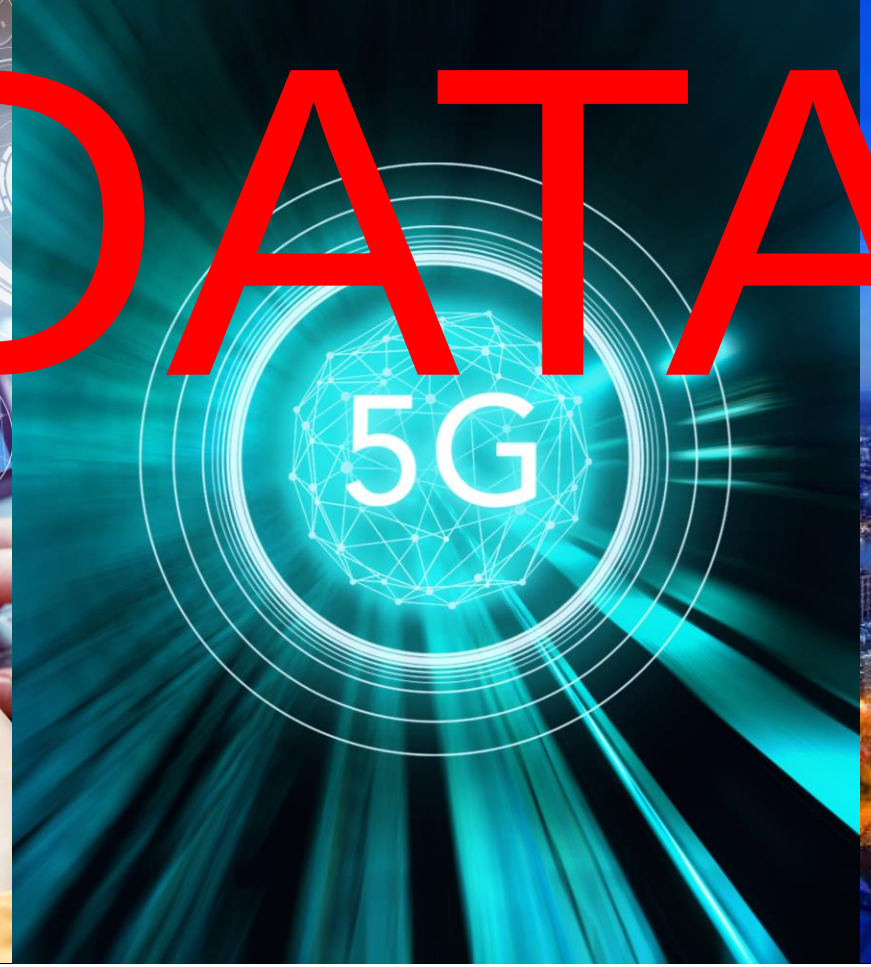
# DATA




**Sensors & Edge Computing**

**5G / Wireless Communications**

**Cloud / Datacenter**

## Pervasive AI enablement



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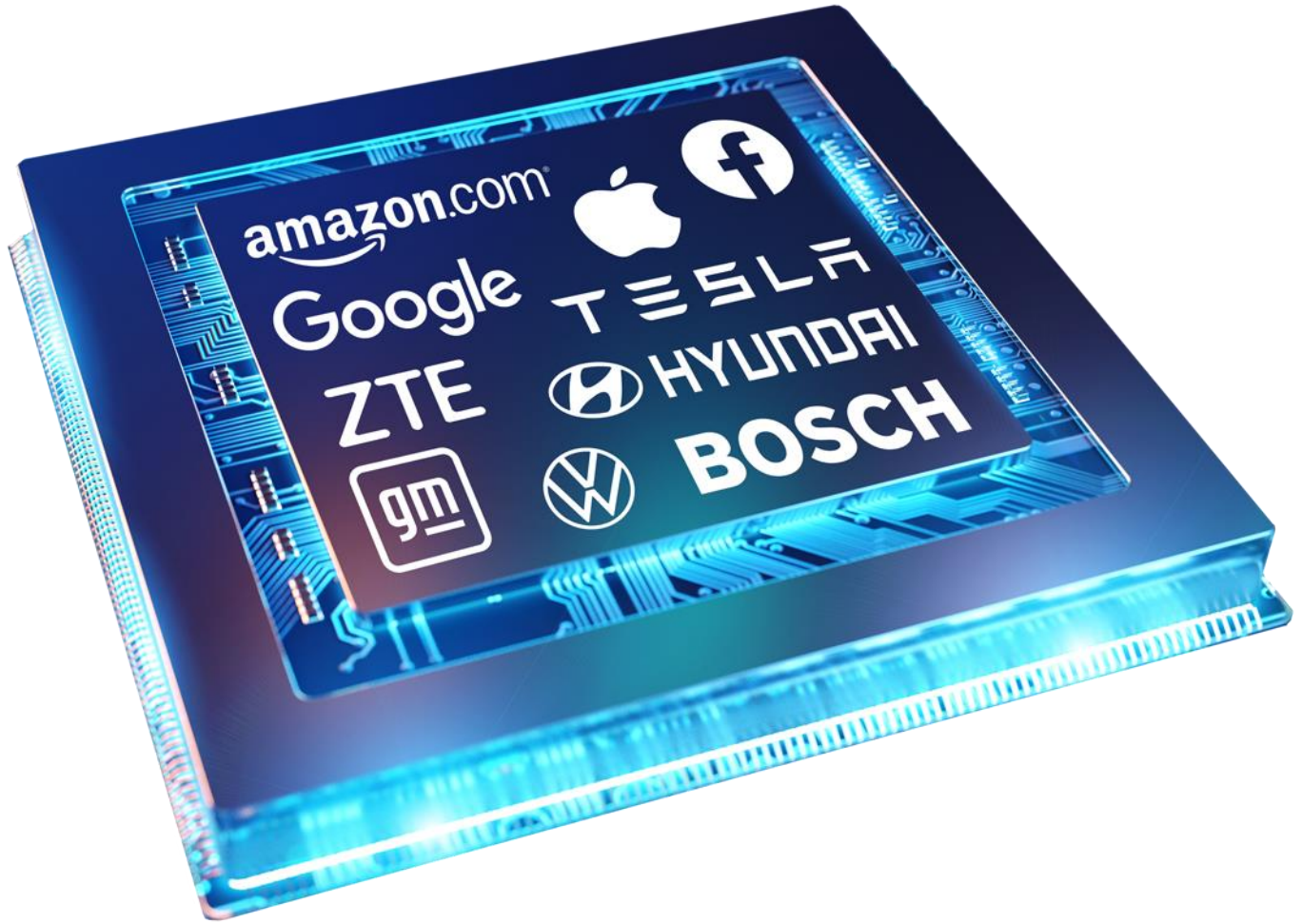
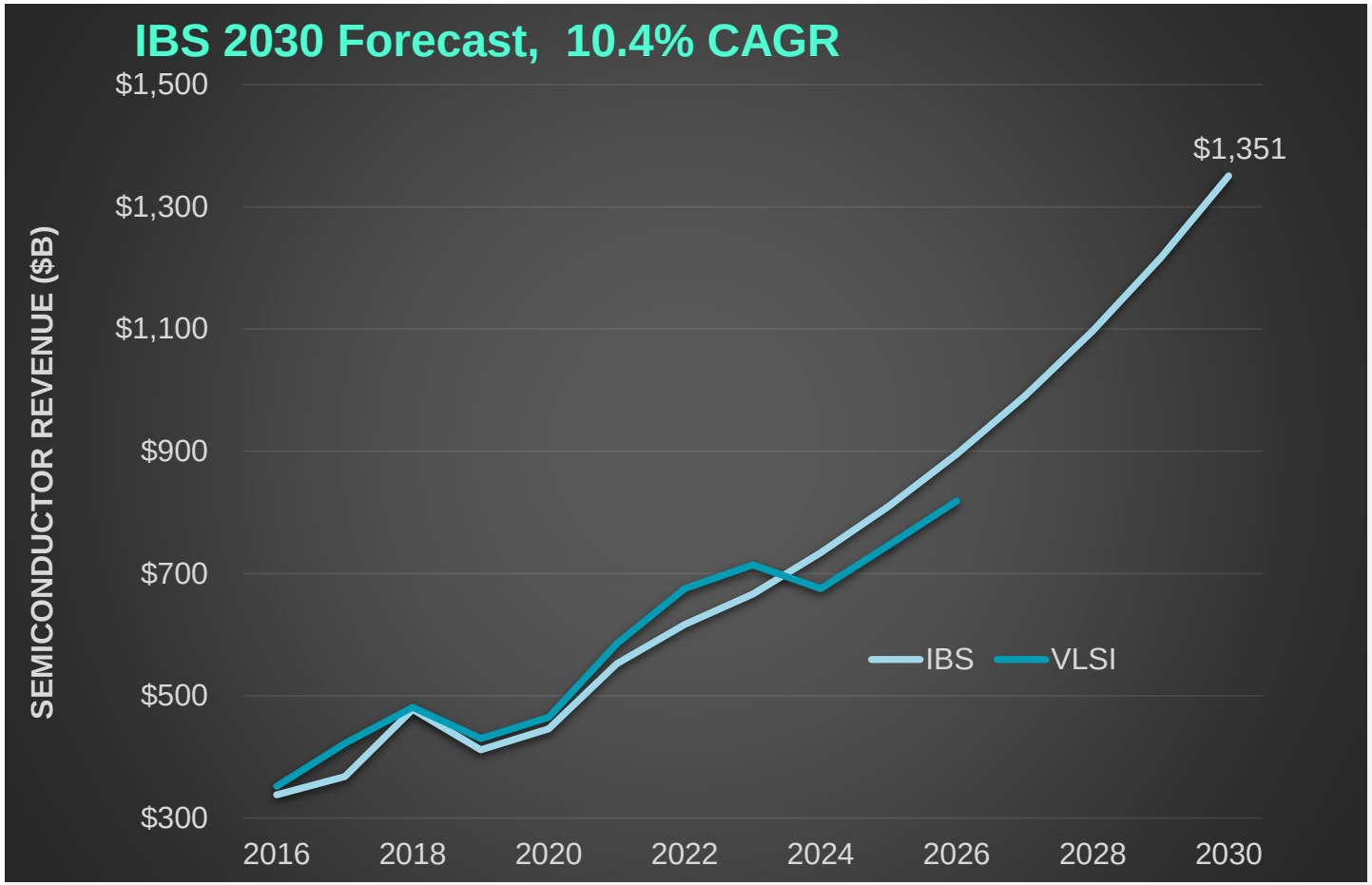
# From systems to ecosystems: Leading edge systems companies are becoming SoC designers, system designers, software designers, enclosures...



# Semiconductors and electronics innovation are the drivers of digitalization; the rapid deployment of cloud, 5G, and edge computing will fuel spectacular growth




Semiconductor industry potentially a **$1 trillion market** by 2030

*Source: International Business Strategies (IBS), January 2022*
*VLSI Research, March 2022*



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# Open-Source EDA

- Ecosystems
  - **RISC-V International (Linux Foundation activity)** www.riscv.org
  - Chips Alliance https://chipsalliance.org/
  - Free Silicon Foundation https://f-si.org/
  - **OpenHW Group (Eclipse Foundation activity)** https://www.openhwgroup.org/
  - Open Source Hardware Association https://www.oshwa.org/
  - OpenROAD's OpenLane https://theopenroadproject.org/
  - Open Source FPGA Foundation https://osfpga.org/
- Interface protocols
  - Generally, membership-only specifications
- Government Agencies
  - United States DARPA https://www.darpa.mil/work-with-us/darpa-toolbox-initiative
  - European Processor Initiative https://www.european-processor-initiative.eu/
  - Digital India RISC-V Microprocessor Program https://shakti.org.in/

# RISC-V Captures Industry's Interest

## Who is RISC-V

**RISC-V International is a global nonprofit association based in Switzerland. Founded in 2015 as the RISC-V Foundation with 29 members, RISC-V is now a truly global organization with 2k+ members in more than 70 countries.**

RISC-V supports the free and open RISC instruction set architecture and extensions delivering a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

RISC-V is part of the Linux Foundation, bringing the community together to build and maintain the open RISC-V ISA.

RISC-V

## Disruptive **Technology**

| Barriers | Legacy ISA | RISC-V ISA |
|---|---|---|
| Complexity | 1500+ base instructions<br>Incremental ISA | 47 base instructions<br>Modular ISA |
| Design freedom | $$$ – Limited | Free – Unlimited |
| License and Royalty fees | $$$ | Free |
| Design ecosystem | Moderate | Growing rapidly. Numerous extensions, open & proprietary cores |
| Software ecosystem | Extensive | Growing rapidly |

RISC-V

# RISC-V Captures Industry's Interest

## Who is RISC-V

**RISC-V International is a glob**
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**members in more than 70 co**

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delivering a new level of free, exte
architecture, paving the way for th

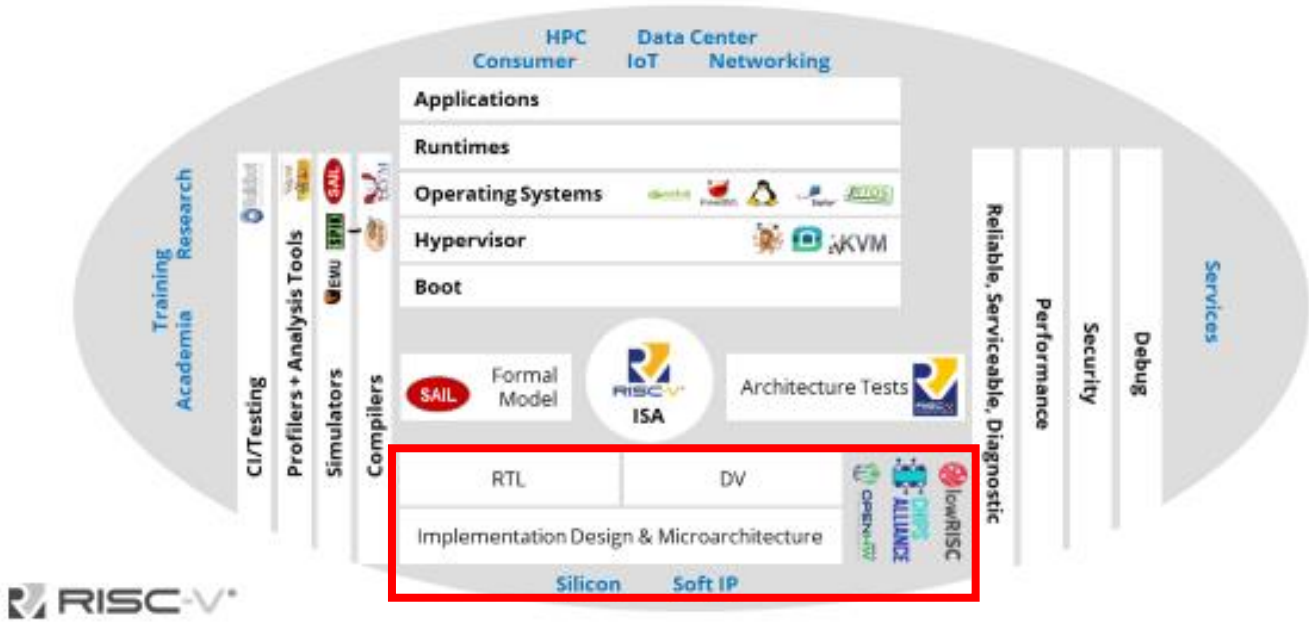
RISC-V is part of the Linux Foundation, bringin

RISC-V

## Disruptive **Technology**

| RISC-V ISA |
| --- |
| 47 base instructions<br>Modular ISA |
| Free – Unlimited |
| Free |
| Growing rapidly. Numerous extensions, open & proprietary cores |
| Growing rapidly |

## RISC-V Ecosystem




RISC-V



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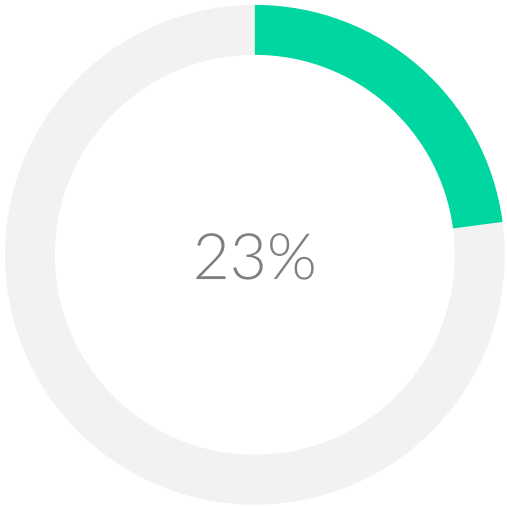
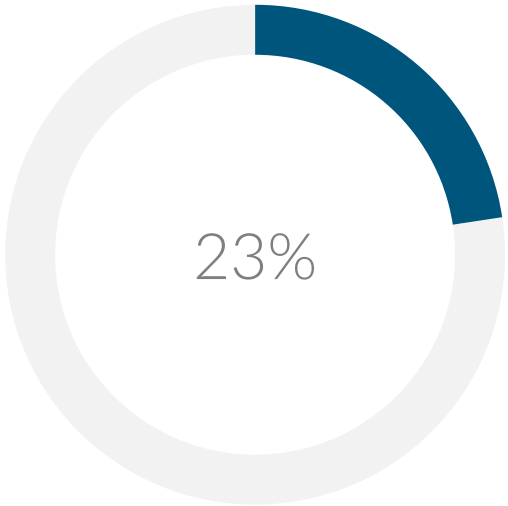
# Projects Incorporating RISC-V Processors in Design

## FPGA




Percentage of FPGA designs that contain a RISC-V processor in the design.

## ASIC/IC




Percentage of ASIC/IC designs that contain a RISC-V processor in the design.

*Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study*

# Open HW Group: Member-driven focus to may Risc-V less Risky

**Mission**

- OpenHW Group is a not-for-profit, global organization driven by its members and individual contributors where hardware and software designers collaborate in the development of open-source cores, related IP, tools and software. OpenHW provides an infrastructure for hosting high quality open-source HW developments in line with industry best practices.

**Core Selection**

- ETH Zurich PULPino (Risc-V Core)
  work done in conjunction with University of Bologna
- “Industrial grade” UVM verification environment

**Related IP**

- In progress

**Tools**

- Commercial & Open Source
  - Siemens Formal Verification

# Open-Source EDA

- Ecosystems
  - **RISC-V International (Linux Foundation activity)** www.riscv.org
  - Chips Alliance https://chipsalliance.org/
  - Free Silicon Foundation https://f-si.org/
  - **OpenHW Group (Eclipse Foundation activity)** https://www.openhwgroup.org/
  - Open Source Hardware Association https://www.oshwa.org/
  - OpenROAD's OpenLane https://theopenroadproject.org/
  - Open Source FPGA Foundation https://osfpga.org/
- Interface protocols
  - Generally, membership-only specifications
- Government Agencies
  - United States DARPA https://www.darpa.mil/work-with-us/darpa-toolbox-initiative
  - European Processor Initiative https://www.european-processor-initiative.eu/
  - Digital India RISC-V Microprocessor Program https://shakti.org.in/

# Thank you

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